2015

A graphical method for determining the uniqueness of operating points in self-biasing circuits

Shiya Liu
Iowa State University

A graphical method for determining the uniqueness of operating points in self-biasing circuits

by

Shiya Liu

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering
Program of Study Committee:
Randall Geiger, Major Professor
Degang Chen
Nicola Elia

Iowa State University

Ames, Iowa

2015

DEDICATION

To my Parents

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AMS	Analog/Mixed-signal
AC	Small signal analysis in the frequency domain
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
PVT	Process-Voltage-Temperature
RMS	Root Mean Square
SoC	System on Chip
SAR	Successive Approximation Register
TSMC	Taiwan Semiconductor Manufacturing Company
VCVS	Voltage Controlled Voltage Source

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere gratitude to my advisor Dr. Randall Geiger for his guidance, motivation, enthusiasm, support and patience. It has been an honor to be his student. Without his guidance, I would never have been able to finish my thesis.

Besides my advisor, I also would like to thank my committee members, Degang Chen and Nicola Elia for their guidance, encouragement, hard questions, and support throughout the course of this research.

In addition, I would also like to thank my friends, colleagues, the department faculty and staff for making my time at Iowa State University a wonderful experience. I want to also offer my appreciation to those who were willing to participate in my surveys and observations, without whom, this thesis would not have been possible.

Finally, I would like to thank my family: Jie Liu, Jiane Li, for giving birth to me and supporting me spiritually throughout my life.

ABSTRACT

In self-biasing circuits, designers often use feedbacks to reduce the power-supply sensitivity and minimize the effects of process and temperature variations. Many self-stabilized circuits are used in SOC circuits even when the SOC has a small amount of AMS content. It is well-known that these self-stabilized circuits are vulnerable to not "starting-up" correctly so start-up circuits are often included to prevent the circuit from getting stuck in an undesired stable operating point. Determining the uniqueness of an operating point in a circuit is challenging since circuit simulators only give a single operating point rather than all operating points. Moreover, this problem is very closely related to the mathematical problem of finding all solutions to a set of nonlinear equations. Both the mathematical and computer science communities recognize this as an open problem with no solution in sight. In circuits with multiple operating points, when a circuit simulator always gives the desired operating point throughout the design and verification process, there is little evidence that one or more undesired operating points even exist. In the semiconductor industry, designers use experience and intuition to identify start-up problems. Some self-stabilized circuits designed by trusted engineers unpredictably get stuck in an undesirable operating point. Engineers often attempt to verify start-up effectiveness with transient simulations. This approach is heuristic and time consuming. Moreover, multiple operating points may still exist in circuits.

All circuits we have studied with known need for start-up circuits have a positive feedback loop (PFL) as part of the self-stabilization process. As a result, we made a conjecture that, "A circuit is vulnerable to the multiple operating points problem only if the circuit has one or more Positive Feedback Loops." A graphical method for identifying positive feedback loops in analog circuits is presented for the purpose of identifying the stable equilibrium points. Firstly, since our

method is based on graphical concepts, some key terminologies from graph theory will be reviewed. Secondly, Graphical models for key analog components are developed and then hierarchically used to obtain a graphical representation of an analog circuit. Thirdly, the concept of determining positive feedback loops from the small-signal resistive Directed, Weighted, Multi-Graph (DWM Graph) of a circuit will be addressed. The three-step process will be used to determine the positive feedback loops. Lastly, a method for breaking positive feedback loop and how to apply the homotopy method to create a return map for the positive feedback loop is introduced. By breaking the positive feedback loop in the circuit and applying break-loop homotopy method, it can determine the uniqueness of operating points in self-biasing circuits.

Sample-and-hold circuit is wildly used in mixed-signal circuits such as data converters, filters etc. Thermal noise is often a design limitation in mixed-signal designs. Many literatures and analog textbooks state that the thermal noise voltage sampled on a capacitor is $\sqrt{kT/C}$ where k is Boltzmann constant, T is temperature and C is capacitance [21][24].

From the expression of thermal noise voltage, we can find that thermal noise is highly related to the capacitor values and independent of resistors. The only way to reduce thermal noise voltage is to increase the capacitance. However, a large capacitor increases the settling time and reduce sampling rate. Meanwhile, layout area and power dissipation will be increased. There is a tradeoff between settling time and accuracy. No literatures introduce a method for reducing thermal noise without increasing capacitance. Reducing noise on a sampling capacitor below $\sqrt{kT/C}$ may give designers opportunities for improving system performance. A method for reducing thermal noise voltage on a sampling capacitor dramatically below $\sqrt{kT/C}$ is introduced.

In high resolution SAR ADC design, many papers state that the minimum capacitance of capacitor DAC is determined by the thermal noise limitation. This thermal noise limitation is kT/C where k is Boltzmann constant, T is temperature and C is the total capacitance of capacitor DAC. Moreover, they assume this is the input-referred noise for the whole ADC. However, this calculation ignores the noise from charge-redistribution mode completely. Meanwhile, no literatures introduce any method about numerical calculation of thermal noise from charge-redistribution mode of capacitor DAC of SAR ADC. A numerical calculation of thermal noise from charge-redistribution mode of capacitor DAC of SAR ADC is introduced.

CHAPTER 1

INTRODUCTION

1.1 Thesis Structure

From chapter 2 to chapter 5, an algorithm for identifying positive feedback loops in self-biasing circuits in order to determine the uniqueness of operating point is discussed. In chapter 2, we will give an introduction of our algorithm for determining the uniqueness of operating points. In chapter 3, we will introduce the method how to identify positive feedback loops. For chapter 4, a method for breaking the positive feedback loops and how to use homotopy method to create a return map is introduced. We will give a summary and examples of our algorithm in chapter 5.

We will move to thermal noise in sample-and-hold circuits in chapter 6. In this chapter, a method for reducing thermal noise voltage on a sampling capacitor dramatically below $\sqrt{k\,T\ /\ C}$ is introduced. We use a switched-capacitor circuit as an example to present how to apply our method to some applications.

In chapter 7, a numerical calculation of thermal noise from charge-redistribution mode of capacitor DAC of SAR ADC is introduced.

CHAPTER 2

INTRODUCTION TO THIS ALGORITHM

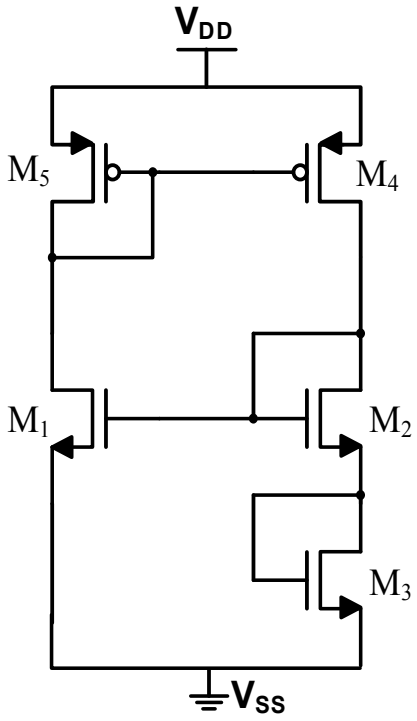
2.1 Motivation

Self-stabilization or "bootstrapping" is a widely used approach for reducing sensitivity of AMS circuits to PVT variations. Designers often use feedbacks to reduce the power-supply sensitivity and minimize the effects of process and temperature variations. Many self-stabilized circuits are used in SOC circuits even when the SOC has a small amount of AMS content. Use of self-stabilization methods will increase as device performance degrades in emerging processes, headroom shrinks, and system performance expectation is enhanced. It is well-known that these self-stabilized circuits are vulnerable to not “starting-up” correctly so start-up circuits are often included to prevent the circuit from getting stuck in an undesired stable operating point. Determining the uniqueness of an operating point in a circuit is challenging since circuit simulators only give a single operating point rather than all operating points. In circuits with multiple operating points, when a circuit simulator always gives the desired operating point throughout the design and verification process, there is little evidence that one or more undesired operating points even exist. Even experienced design teams of top semiconductor companies reluctantly report numerous examples of circuit start-up failures that were detected experimentally at testing or first discovered from customs returns. Design teams with decreasing AMS design experience will become increasely vulnerable to start-up problems.

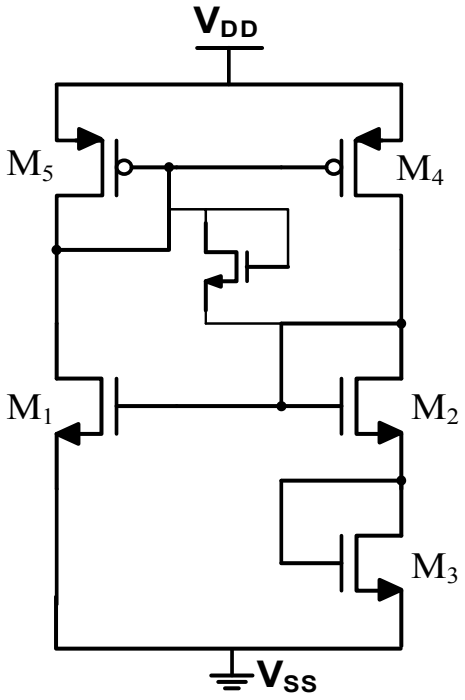
Although the issue of start-up circuits arose naturally because of problems designers experienced by inadvertently creating undesired stable equilibrium points in a circuit, accidental or adversarial introduction of undesired stable equilibrium points creates vulnerability for the introduction of Trojan states in a circuit that can be extremely difficult to detect. The

consequences of the presence of a Trojan state on a mission-critical or trusted communication link in military systems could be disastrous. By exploiting this gateway that exists or that can be inconspicuously created in most large SoC scale integrated circuits, concerns about trust in electronic circuits naturally arise. Methods of verifying that a circuit is free of Trojan Operating States are needed if trusted electronic circuits are to be obtained from untrusted sources.

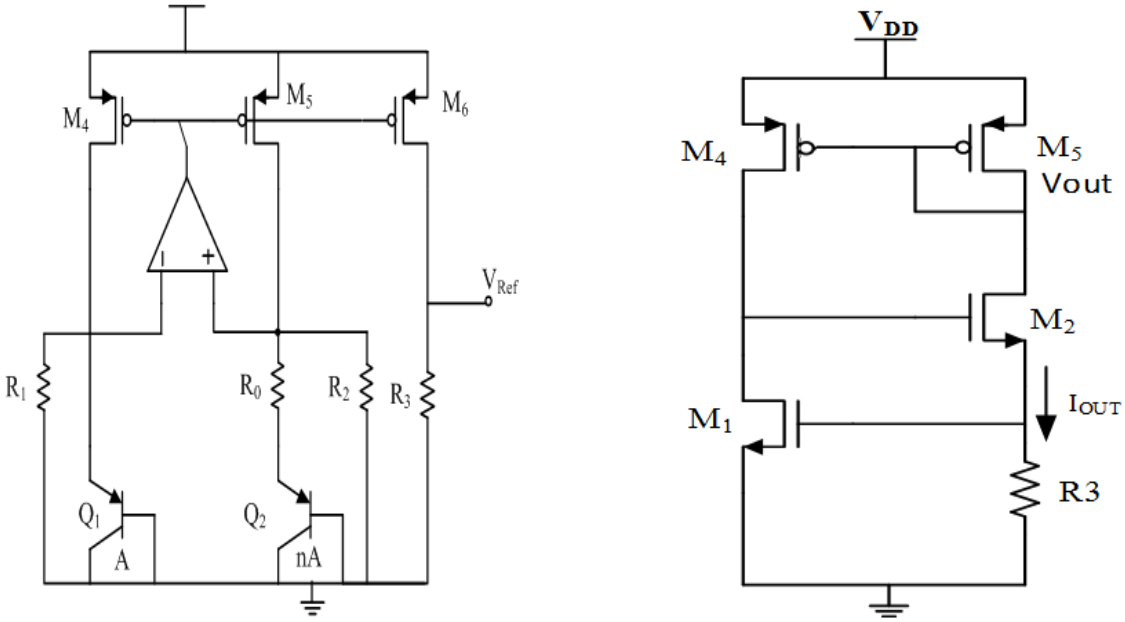
There are many different circuits that use self-stabilization to reduce supply sensitivity. Four examples of self-stabilized circuits are shown in Fig. 2.1.



(a)



(b)



(c) (d)

Figure 2.1 Self-Stabilized Circuit Examples (a) An Inverse-Widlar Circuit without a Start-Up Circuit (b) An Inverse-Widlar with a Start-Up Circuit (c) A Banba Bandgap Reference (d) A Wilson Bias Generator

2.2 Traditional Approach

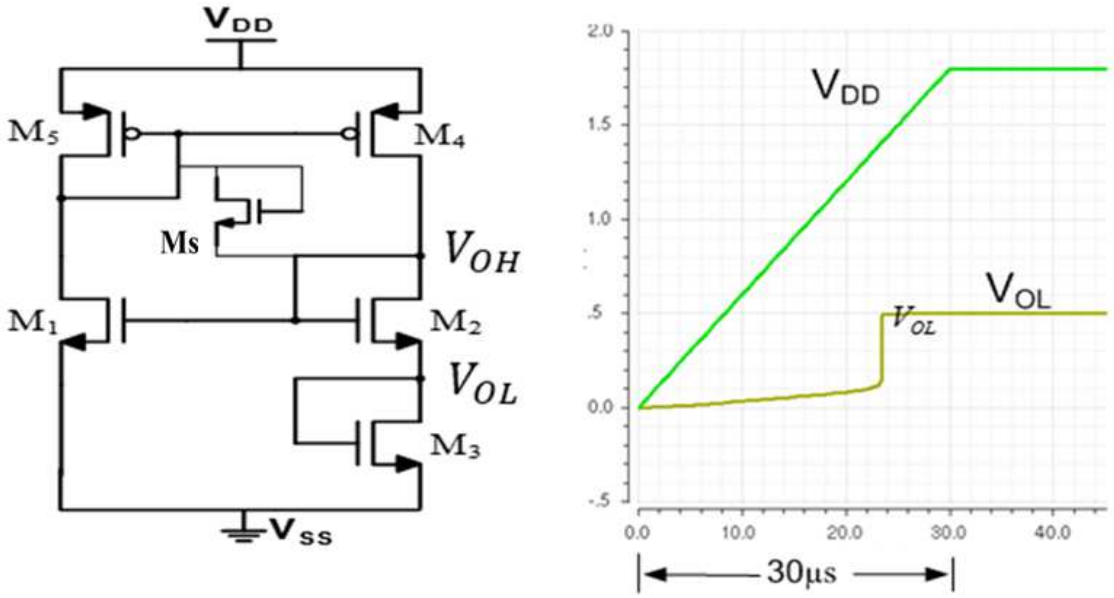
Generally, designers use experience and intuition to identify start-up problems. Some self-stabilized circuits designed by trusted engineers unpredictably get stuck in an undesirable operating point. Circuit simulators provide only one solution to a nonlinear circuit. Trojan States can be missed throughout the entire design and verification process even with the use of the best available tools. Determining the uniqueness of an operating point is very closely related to the mathematical problem of finding all solutions to a set of nonlinear equations. Both the mathematical and computer science communities recognize this as an open problem with no solution in sight. In the semiconductor industry, engineers often attempt to verify start-up effectiveness with transient simulations. This approach is heuristic and time consuming.

Moreover, multiple operating points may still exist in circuits even when a start-up circuit passes standard transient-simulation based start-up verification tests.

Consider an Inverse-Widlar bias generator with a start-up circuit as an example. The circuit is depicted in Fig. 2.2(a). A standard start-up verification procedure involves simulating the circuit with a slow ramp on the supply voltage. With this approach, the steady-state value of an output voltage is compared with the desired output voltage. If the desired value agrees with the value obtained with the transient simulation, the circuit passes the start-up verification and circuit is assumed to be effective. If the transient simulation does not agree with the desired operating point, it is concluded that the start-up circuit is not effective. In Fig. 2.2, V_{DD} and the designed value of V_{OL} are 1.8V and 0.5V respectively. The transient response for this circuit is shown in Fig. 2.2(b). With the start-up circuit, V_{OL} converges to the designed value and thus it is concluded that the start-up circuit is effective. device sizes are shown in Table 1. This simulation is in TSMC 0.18um process with a 1.8 V power supply.

Table 2.1 Device Sizes of Circuit

Transistor	Width(um)	Length(um)	Multiples
M1	0.3	0.9	1
M2	5	0.3	2
M3	7	0.3	2
M4	0.56	0.3	2
M5	0.5	0.72	6
Ms	0.5	0.72	6



(a) (b)

Figure 2.2 (a) An Inverse-Widlar Circuit with a Start-Up Circuit (b) Transient Response of the Inverse-Widlar Circuit

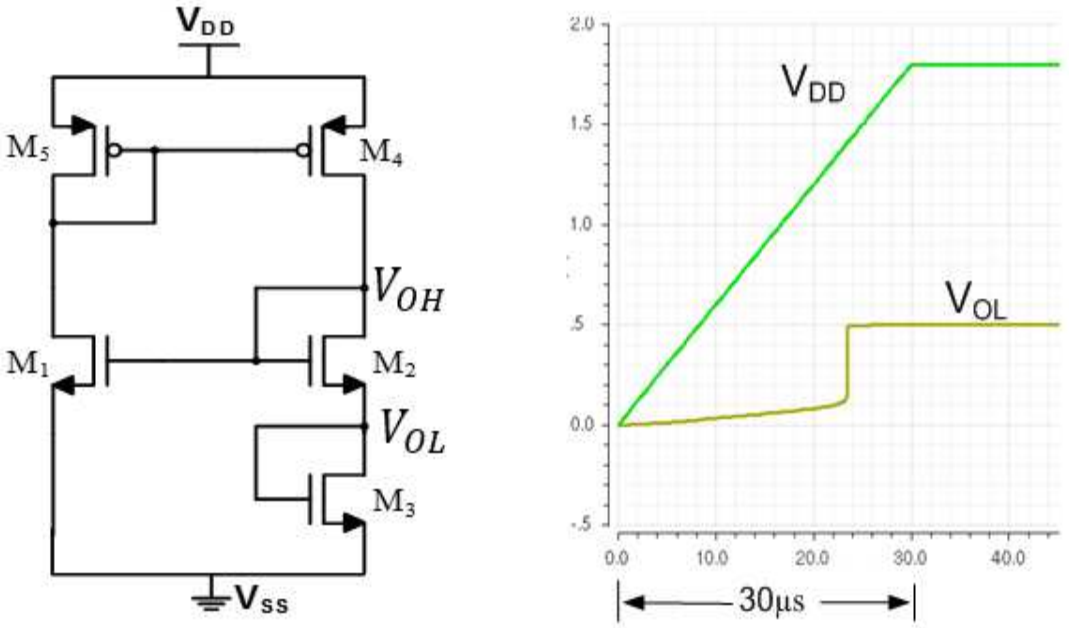
Consider now the same Inverse-Widlar bias generator but without a start-up circuit as an example. This circuit is known to have two Trojan operating points. The circuit is depicted in Fig. 2.3(a). The transient response for this circuit is shown in Fig. 2.3(b). Since the output from the transient simulation converges to the desired output, the circuit passes the transient simulation test and it is thus incorrectly concluded that the circuit has one operating point. The three operating points of two node voltages, V_{OL} and V_{OH}, are shown in Table 2. From this example, we can find that transient simulation cannot determine the uniqueness of operating points. device sizes are shown in Table 3. This simulation is in TSMC 0.18um process with a 1.8 V power supply.

Table 2.2 Operating Points of Nodes V_{OL} and V_{OH}

Voltage	Operating Point 1	Operating Point 2	Operating Point 3
V_{OL}	0.5V	80mV	7mV
V_{OH}	1.16V	0.2V	18mV

Table 2.3 Device Sizes of the Circuit

Transistor	Width(um)	Length(um)	Multiples
M1	0.3	0.9	1
M2	5	0.3	2
M3	7	0.3	2
M4	0.56	0.3	2
M5	0.5	0.72	6



(a) (b)

Figure 2.3 (a) An Inverse-Widlar Circuit without a Start-Up Circuit (b) Transient Response of the Inverse-Widlar Circuit

2.3 Conjecture

Some methods have been proposed to determine the uniqueness of DC operating points [1][3][6][7]. However, these methods are not practical even for circuits with a very small number of devices due to excessive computing requirements. In reference [1], author Alan Willson observed that for circuits with bipolar transistors, "…any transistor circuit whose DC equations have more than one solution must have a topological substructure like that of Fig. 1 embedded somewhere within its overall topology". The circuit referred by Willson is shown in Fig. 2.4. Though the issue of "positive feedback" was not specifically addressed by Willson, the structure of Fig. 2.4 is a positive feedback circuit and all circuits the authors have studied with known

need for start-up circuits have positive feedback loops as part of the self-stabilization process. With these observations, the following conjecture is made:

Conjecture:

A circuit is vulnerable to the Trojan state problem only if the graph representation of circuit has one or more positive feedback loops.

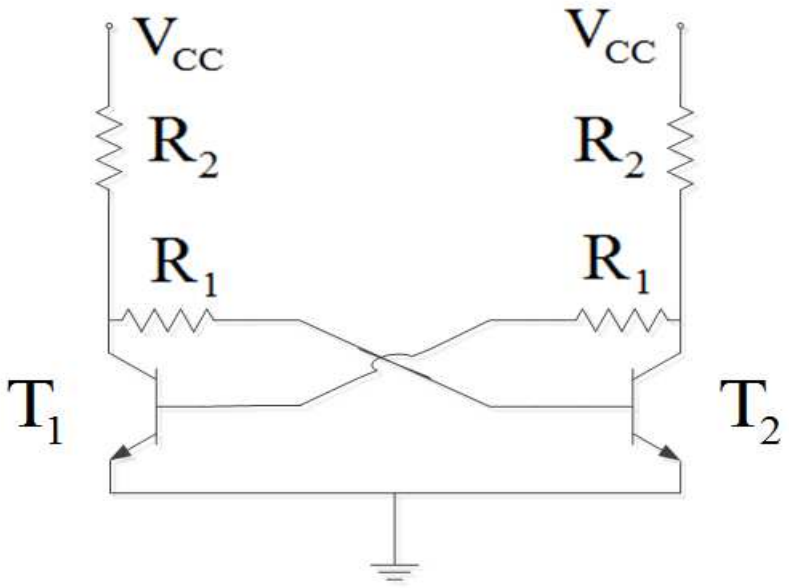


Figure 2.4 The Feedback Circuit from Alan Willson's Paper

A vulnerable circuit may not actually have a Trojan state but if the circuit is not vulnerable, the concern of a Trojan state vanishes. There are some reported methods for identifying positive feedback loops but most are matrix-oriented. A method for identifying positive feedback loops from a graphical representation of a circuit is introduced here. With this method, graphical models for key analog components are given and a general method for converting the circuit to a graph using these component models is presented. Emphasis will be restricted to circuits that have a single positive feedback loop though the concepts can be extended to circuits that have two or more positive feedback loops.

Though the concept of a positive feedback loop is widely discussed in the context of electronic circuits and control systems, a rigorous definition of the concept, particularly in nonlinear circuits with non-unilateral coupling between devices, is seldom given. There are numerous graphical representations of a circuit that have been used in the past for different purposes. Some are developed for representing connectivity in physical design. Others are used to represent signal flow in a circuit whereas others may be useful for identifying nodes or meshes for circuit analysis. Often graphical representations are used to obtain significant simplifications of a circuit or a system at the expense of some loss of information. In the graphical representation that be developed here, the goal will be to preserve the feedback loop structure in the circuit including the sign of the loop gain in a simple graphical representation of the circuit while suppressing many details about the circuit itself. By focusing on a simple graphical representation that suppresses many details about the circuit itself, there is a small risk that some positive feedback loops will be missed or that the sign of a feedback loop may be misclassified. However, in numerous examples of circuits that were considered, the method that will be described has proven effective at identifying the presence or absence of static Trojan operating states.

2.4 Our Method

The procedure of proposed method can be described as the following. Initially structural issues in circuits that are indicative of potential Trojan state problems will be identified. In order to determine if a circuit is structurally vulnerable to Trojan state, our goal is to create a graph that captures feedback mechanisms from a circuit schematic. In the second part of this process, positive feedback loops will be identified from the graphical representations of a circuit. The

process is automatable and computationally practical. In the last part of this process, homotopy methods will be applied to the positive feedback loops that have been identified in a circuit to verify whether a circuit has multiple operating points.

2.5 Basic Graph Theory Concepts

Since our method is based on graphical concepts, some key terminologies from graph theory will be reviewed in this section. Standard notation for the concepts of an ordered pair and a sequence of real numbers will be adopted [12][13].

Distinct Ordered Pairs

Ordered pairs A_1=(a,b) and A_2=(c,d) are termed distinct if $a \neq c$ or $b \neq d$.

Graph

A graph G is a pair of finite sets (V, E) where the elements in V are termed nodes and the elements of E are distinct ordered pairs of nodes in V termed edges.

Weighted Edge

A weighted edge of a graph is an ordered triple (b_K, b_L, r) where (b_K, b_L) is an edge of the graph and r is a real number.

Directed, Weighted, Multi-Graph (DWM Graph)

A Directed, Weighted, Multi-Graph, G, is a pair of sets (V, B), where V is a finite set of nodes, and B is a finite set of weighted edges (b_K, b_L, r) where $b_K, b_L \in V$.

Sub-DWM Graph

A sub-DWM Graph of a DWM Graph G = (V, B) is a graph G' = (V', B') such that V' ⊂ V, B' ⊂ B.

Element DWM Graph (EDWM Graph)

For key analog components such as, transistors, diodes, resistors, etc. there is a DWM Graph corresponding to each of them. A DWM Graph corresponding to an element in a circuit is called an Element DWM Graph. Mapping of specific circuit elements to an EDWM Graph will be discussed later.

Walk

A walk in a DWM graph G = (V, B) is a sequence of the form

$$(v_1,(v_1,v_2,r_{1,2}),v_2,(v_2,v_3,r_{2,3}),v_3,\ldots,v_k,(v_k,v_{k+1},r_{k,k+1}),v_{k+1})$$

where $k \geq 0$, $v_i \in V$ and $\{v_i, v_{i+1}, r_{i,i+1}\} \in B$ for $1 \leq i \leq k$.

Length of walk

The length of a walk is the number of weighted edges in the walk.

Loop

A loop in a DWM Graph G = (V, B) is a walk of length $k \geq 1$ in which elements $v_1, \ldots, v_k$ of V are distinct and $v_1 = v_{k+1}$.

Length of Loop

The length of a loop is the number of weighted edges in a loop.

Weight of Loop

The weight of a loop G, where G is a sequence of the form

$$(v_1,(v_1,v_2,r_{1,2}),v_2,(v_2,v_3,r_{2,3}),v_3,...,v_k,(v_k,v_{k+1},r_{k,k+1}),v_{k+1})$$

is

$$W=\sum_{i=1}^{k} r_{i,i+1}$$

Union Graph

Consider a set of DWM Graphs $\{G_1(V_1,B_1),G_2(V_2,B_2),G_3(V_3,B_3),.....,G_k(V_k,B_k)\}$

The Union Graph G (V, B) of this set of DWM Graphs is defined by

$$V=\bigcup_{i=1}^{k} V_i$$

and

$$B=\bigcup_{i=1}^{k} B_i$$

The elements in $\{V_1,V_2,\ldots V_k\}$ can be unique or the individual node sets may have one or more nodes in common. A Union Graph is also a DWM Graph.

2.6 Traditional Method for Mapping Circuits to Graphs

In the previous section, the graphical representations were formally given as a relationship between sets of vertices and ordered pairs or ordered triples. Often a visual depiction of a graph is used instead of the more formal notation. A Node Link Diagram is a pictorial representation of a DWM Graph. In the Node Link Diagram, vertices are represented by dots or circles with

labelled with the labels of the vertices in the DWM Graph. Edges in the DWM Graph are represented as lines or arcs connecting the corresponding vertices with an arrow on the vertex corresponding to the second node in the ordered pair defining the edge. The weight of the edge is represented by a number placed adjacent to the line or arc.

There are several methods for mapping a circuit to a graph, some of which are discussed in references [29][30][31][32]. The mapping of a two-terminal element in Narsingh Deo's book "Graph Theory with Applications to Engineering and Computer Science" [29] is described as "A two-terminal electrical element is represented by an edge e_k. Associated with each edge are two edge variable, $v_k(t)$ and $i_k(t)$." Fig. 2.5 shows the Node Link Diagram of the graphical model of a two-terminal electrical element from this book.

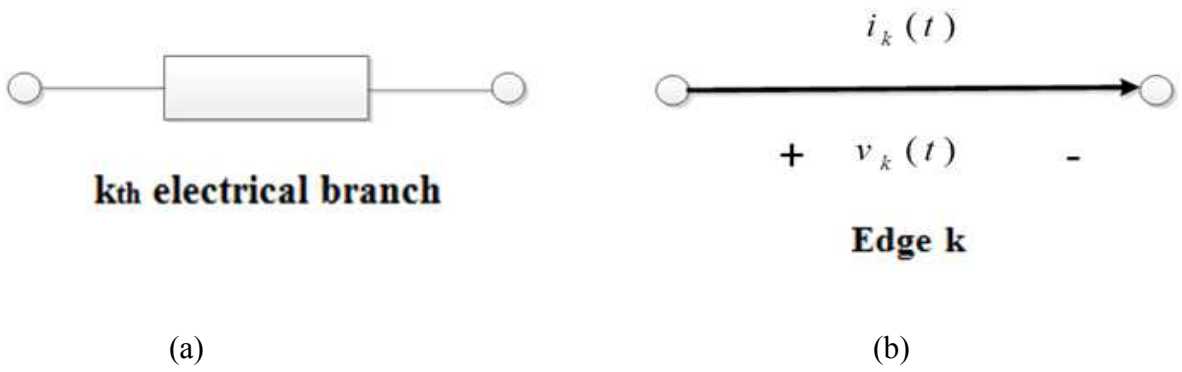
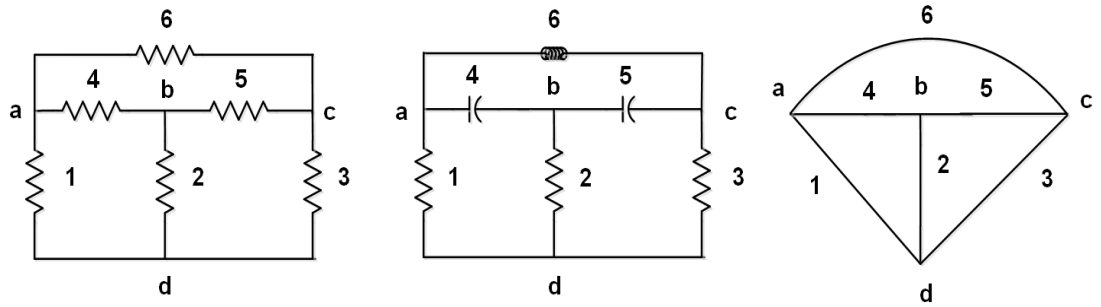


Figure 2.5 (a) A Two-Terminal Electrical Element (b) Node Link Diagram of Graph Model of a Two-Terminal Electrical Element

This mapping preserves both current and voltage information about the element and the direction is based upon the passive sign convention. In another book [30] titled "Circuit Theory", the author states that "When R, L and C elements and sources like V_s and I_s are connected appropriately, an electrical circuit results. The elements and sources have two end-points each. They are thus 'two-terminal elements'. The connection points of elements and

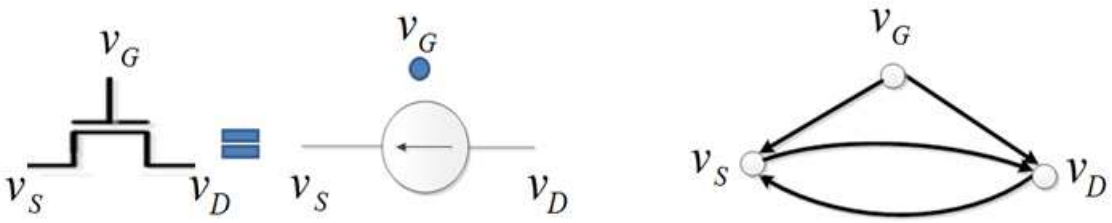
sources are called nodes." Fig. 2.6 shows an example from this book for mapping from circuits to graphs. The author states that, "Figure 4.1(a) and (b) shows two different basic networks and Fig. 4.1(c) their graph G which is the same for the two networks. The graph in Fig. 4.1(c), as well as the electrical network it represents, consists of four nodes, a, b, c and d and six branches 1 to 6." The figure referred by the author is shown in Fig. 2.6. In this mapping, nodes in the circuit are mapped distinctly to vertices in the graphical representation. This mapping preserves topological information but suppresses information about the characteristics of the circuit elements themselves.



(a) (b) (c)

Figure 2.6 (a) A Electrical Circuit (b) A Electrical Circuit (c) Graph of These Two Circuits

In book, "Circuit Simulation Methods and Algorithms"[33], the author creates a dependency graph for circuit and uses directed edges for representing the dependence between each nodes. The author states that "if the i_{th} component is dependent on solution of the j_{th} components, then the dependency matrix A has the element $a_{ij} = 1$. Equivalently, we can draw the signal-flow graph, with as many vertices as there are components in the circuit, and set in this graph a directed edge from j to i for each pair of dependent components." The dependence graph for MOS transistor from the book is shown in Fig. 2.7.



(a) (b)

Figure 2.7 (a) A MOS Transistor (b) Dependence Graph for a MOS Transistor

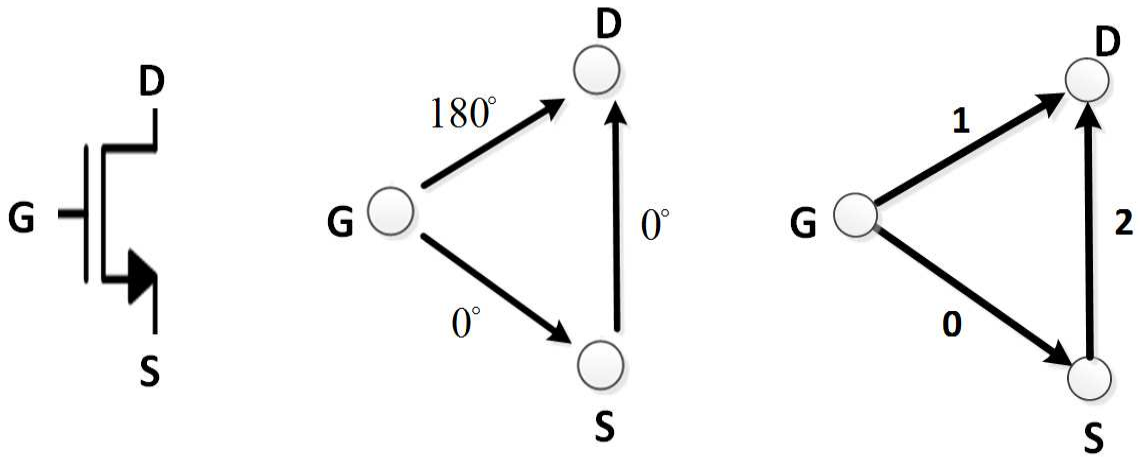
Taking nodes v_D and v_S as an example. For node v_D, there are two edges point to this node from v_G and v_S respectively. It means that signal at v_D is dependent on v_G and v_S. For node v_S, there are also two edges point to this node from v_D and v_G respectively. It means that signal at v_S is determined by signals at v_G and v_D.

In lecture notes [32], Allen depicted signal flow information in a transistor as shown in Fig. 2.8. Others have followed similar approaches in the past. Though Allen did not use a normal graphical representation, his signal flow information suppresses detailed information about the transistor and focuses only on whether a signal is inverted or non-inverted as is passed from one node to another in a circuit. The signal flow information approach of Allen is summarized in the Node Link Diagram of Fig. 2.9 (b). Since only phase shift information is captured in Allen's model, it can be modeled by the sign of the signal that propagates from one node to another as shown in Fig. 2.9 (c). The number 1 is used for representing 180 degree phase shift from node G to node D. The number 2 is used for representing 0 degree phase shift from node S to node D. The reason why number 2 is preferred for 0 degree phase shift from node S to node D is that there is actually 360 degree phase shift between these two nodes. The number 0 is used for

representing 0 degree phase shift from node G to node S since there is no 360 degree phase shift between these two nodes.

(a) (b)

Figure 2.8 (a) Signal Flow in BJT (b) Signal Flow in MOS Transistor



(a) (b) (c)

Figure 2.9 (a) A MOS Transistor (b) Node Link Diagram of a MOS Transistor (c) Graphical Representation of a MOS Transistor

As can be seen by these examples of mapping a circuit to a graph, some information is suppressed and, in the case of the signal flow graph of Allen, most of the information is suppressed. But Allen's approach is attractive in the sense that the graphical representation is

simple. There is a one-to-one correspondence between nodes in the circuit and vertices in graph, and the concept of signal flow is maintained. By maintaining signal flow information, the signal flow loops or feedback loops should be preserved. One additional observation about the signal flow information obtained in the Allen mapping. If one considers the three basic amplifier configurations, Common Source, Common Drain, and Common Gate, the sign of the signal flow used by Allen corresponds to an inversion between G and D in the Common Source configuration, and a non-inversion between G and S and between S and D for the Common Drain and the Common Gate configurations. However, if several transistors are combined in a circuit, it is possible that the signal flow inversion from G to D in an individual transistor will not occur in the larger circuit and this is due to the severe compression of details about the circuit that accompany the mapping from the transistor to the graphical representation in Fig. 2.9(c).

2.7 Creating a Graph from a Circuit

We now focus on the creation of a DWM Graph from a small-signal resistive circuit. This graphical representation preserves signal flow information but suppresses many of the details about the circuit itself. By preserving signal flow information, feedback loops in the circuit should be preserved in the graphical representation. More importantly, loops in the circuit that are classified as positive feedback loops should be identifiable in the graphical representation.

This is approached by creating a resistive EDWM Graph for each element in a circuit and then creating the Union Graph of all the EDWM Graphs for all elements in the circuit by equating any nodes in the EDWM Graphs that are coincident in the circuit. This Union Graph of all the EDWM Graphs for the circuit is the DWM Graph for the circuit.

Consider a circuit with N nodes, K elements

$$N = \{n_1, n_2, ..., n_k\}$$
$$K = \{K_1, K_2, ..., K_n\}$$

The set of EDWM Graphs corresponding to the n elements is

$\{G_{E1}(V_1, B_1), G_{E2}(V_2, B_2), G_{E3}(V_3, B_3), ..., G_{En}(V_n, B_n)\}$ where nodes in $\{V_1, V_2, \ldots V_n\}$ that are coincident in the circuit are coincident in $V_U = \bigcup_{i=1}^{n} V_i$. The DWM Graph of the circuit is the Union Graph of these n element graphs and is denoted as

$$U = \{V, B\}$$

With this approach, every node in *N* is mapped to a node in V but it is possible that the EDWM Graphs contain additional nodes that are not nodes in the circuit. It is also possible that the EDWM Graphs combine or merge nodes in the original circuit. For the elements that will be considered in this work, however, the EDWM Graphs will introduce no additional nodes. Thus, there will be a one-to-one mapping between nodes in the circuit and vertices in the graphical representation. With this restriction, there will be at most k nodes in V and each node in *N* corresponds to a node in V but some nodes in V may correspond to two or more nodes in *N*.

We now consider circuits comprised of MOS transistors, diodes, resistors, capacitors, inductors, and independent dc voltage or current sources. We will obtain the resistive small-signal EDWM Graph for each of these elements. There may be more than one way to create an EDWM Graph for each element but we will focus on creating a single EDWM Graph for a select set of critical elements.

2.8 Creating EDWM Graph for Circuit Components

Mapping of MOS Transistors

We restrict this mapping to three-terminal models of the devices. Each MOS transistor thus has three terminals denoted as Gate, Drain and Source each of which corresponds to a node in the EDWM Graph. The EDWM Graph for a MOS transistor is denoted as:

$$G_{MOS} = (V, \mathrm{B})$$
$$V = \{G, D, S\}$$
$$B = \{\{G, D, 1\}, \{G, S, 0\}, \{S, D, 2\}\}$$

The EDWM Graph of a MOS transistor is visually depicted by the Node Link Diagram in Fig. 2.10. This is the signal flow mapping used by Allen and depicted in Fig. 2.8.

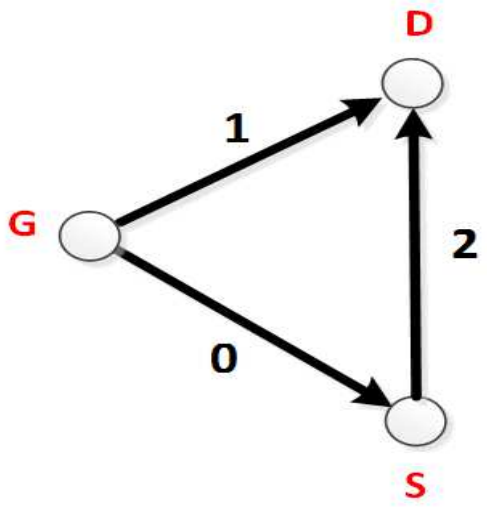


Figure 2.10 Node Link Diagram of EDWM Graph of a Transistor

In this representation, the same symbology will be used for nodes in the circuit element and nodes in the graphical representation of the element. This will facilitate visualization of the mapping between the circuit element and its graphical representation.

Mapping of Diodes

Each diode has two terminals denoted as Anode and Cathode. The EDWM Graph of a diode is denoted as:

$$G_{Diode} = (\mathrm{V}, \mathrm{B})$$
$$V = \{A, C\}$$
$$B = \{\{A, C, 0\}\}$$

The Node Link Diagram of EDWM Graph of a diode is visually depicted in Fig. 2.11.

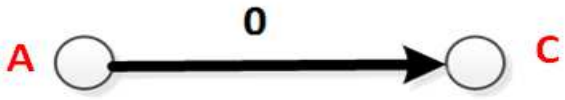


Figure 2.11 Node Link Diagram of EDWM Graph of a Diode

Mapping of Diode-Connected Transistors

MOS transistor has three terminals denoted as Gate, Drain and Source. For diode-connected transistor, Gate and drain are tied together so that there are only two terminals. The EDWM Graph of a diode-connected transistor is denoted as:

$$G_{Diode\_MOS} = (\mathrm{V}, \mathrm{B})$$
$$V = \{\mathrm{G}, \mathrm{S}\}$$
$$B = \{\{\mathrm{G}, \mathrm{S}, 0\}\}$$

The Node Link Diagram of EDWM Graph of a diode-connected transistor is visually depicted in Fig. 2.12.

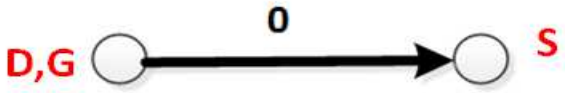


Figure 2.12 Node Link Diagram of EDWM Graph of a Diode-Connected Transistor

Mapping of Resistors

The mapping for the resistor is similar to that of the diode with the distinction that the signal can propagate through the resistor in both directions. This bidirectional signal propagation creates a second branch. Mapping of resistor to an EDWM Graph is denoted as:

$$G = (\mathrm{V}, \mathrm{B})$$
$$V = \{A, \mathrm{C}\}$$
$$B = \{\{A, \mathrm{C}, 0\}, \{\mathrm{C}, A, 0\}\}$$

The Node Link Diagram of EDWM Graph of a resistor is visually depicted in Fig. 2.13. The double arrows in the symbol are used to represent the two branches in the graph.

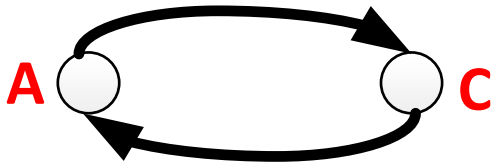


Figure 2.13 Node Link Diagram of EDWM Graph of a Resistor

Mapping of Capacitors and Inductors

Capacitor and inductor don't appear in small-signal resistive circuits. As a result, there is no model for these two components.

Mapping of Independent and Dependent Voltage Sources

Independent voltage sources don't appear in small-signal resistive circuits. So there is no model for this circuit component. Dependent voltage sources are not considered in this work.

CHAPTER 3

IDENTIFICATION OF POSITIVE FEEDBACK LOOP FROM DWM GRAPH OF CIRCUIT

3.1 Determine the Positive Feedback Loops

In this section, the concept of determining positive feedback loops from the small-signal resistive DWM Graph of a circuit will be addressed. A three-step process will be used to determine the positive feedback loops. The first step is the creation of a DWM Graph from the circuit schematic by creating the Union Graph from the EDWM Graph of each element and making the appropriate node associations. This was discussed in chapter 2. The second step involves the creation of a reduced DWM Graph that preserves the positive feedback loops but that facilitates a more practical extraction of the positive feedback loops. The reduced DWM Graph is a subgraph of the DWM Graph. The third step involves identifying the positive feedback loops from the reduced DWM Graph.

G' = (V', B')

Definition of Positive Feedback Loop

A loop G' = (V', B') of a DWM Graph G = (V, B) is a positive feedback loop if and only if the loop satisfies the following conditions:

1) *The length of loop is* ≥ 2.
2) *The weight of the loop is an even number which is larger than or equal to 2.*

After the positive feedback loops are determined, homotopy method is used to determine if the circuit has more than one stable operating point. This involves breaking the positive feedback loops in the graphical representation of the circuit and then breaking the corresponding positive

feedback loops in the circuit in such a way that equilibrium points are not perturbed. Once the positive feedback loops are broken, return maps will be created. Points where the return map equals one are the equilibrium points of the circuit. This overall process can be summarized as follows:

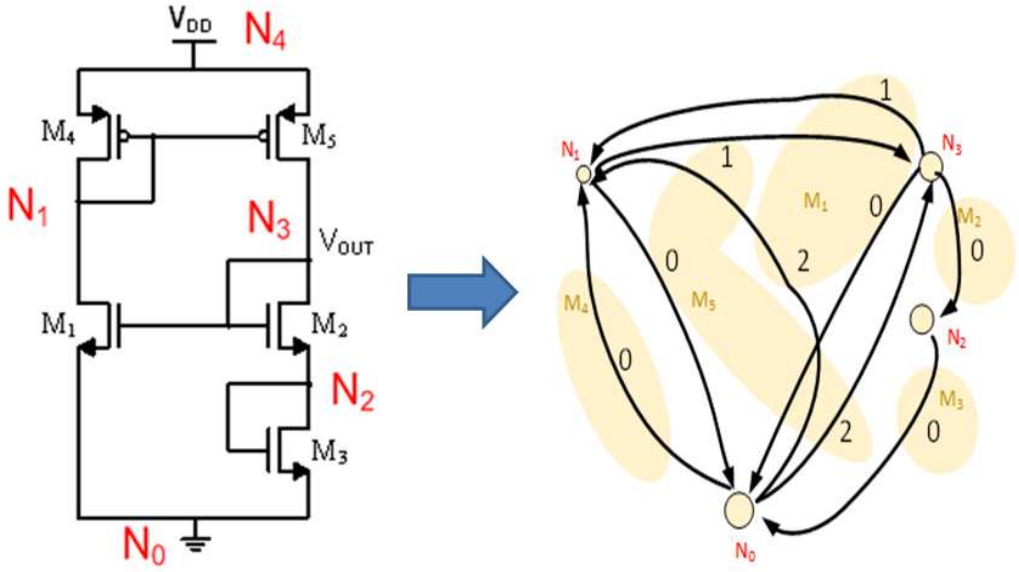
1. Create a DWM Graph of Circuit
2. Create a reduced DWM Graph
3. Identify positive feedback loops from the reduced DWM Graph
4. Break positive feedback loops in the reduced DWM Graph
5. Break corresponding positive feedback loops in the circuit
6. Apply homotopy method to obtain return map
7. Determine equilibrium points from return map

This chapter will focus only on the first three steps in this process by considering examples to demonstrate the process. In the following chapter, the remaining steps in this overall process will be discussed.

3.2 Creation of DWM Graph of Circuit

Consider the Inverse-Widlar bias generator circuit shown in Fig. 3.1(a) as an example to demonstrate this process. In this example, the start-up circuit is not included. Fig. 3.1(b) shows the Node Link Diagram of the DWM Graph of the Inverse-Widlar circuit in Fig. 3.1(a) obtained by creating the Union Graph from the EDWM Graph of each of the five elements. The labels of the vertices in the DWM correspond to the labels for the nodes in the original circuit. Fig. 3.1

(b) shows an intermediate step mapping the individual circuit elements to the corresponding EDWM Graph. Note that nodes N_0 and N_4 are merged into a single node since the independent V_{DD} voltage source is connected between these two nodes in the circuit schematic.



(a) (b)

Figure 3.1 (a) An Inverse-Widlar Circuit without a Start-Up Circuit (b) Node Link Diagram of DWM Graph of an Inverse-Widlar Circuit without a Start-Up Circuit

The second step involves the creation of a reduced DWM Graph. As can be seen from the Inverse-Widlar circuit example, even a simple circuit can have a rather complicated DWM Graph with a large number of branches. This increases the challenges associated with obtaining the positive feedback loops in the DWM graph.

This is based upon the following conjecture:

Conjecture: The subgraph of a DWM Graph obtained by eliminating the ground node and all branches connected to the ground node will have the same positive feedback loops as the original DWM Graph.

It will not be proved that this reduction step preserves all positive feedback loops but in the examples that have been considered, this reduction process has preserved the positive feedback loops. The Node Link Diagram of reduced DWM Graph for the Inverse-Widlar circuit is depicted in Fig. 3.2.

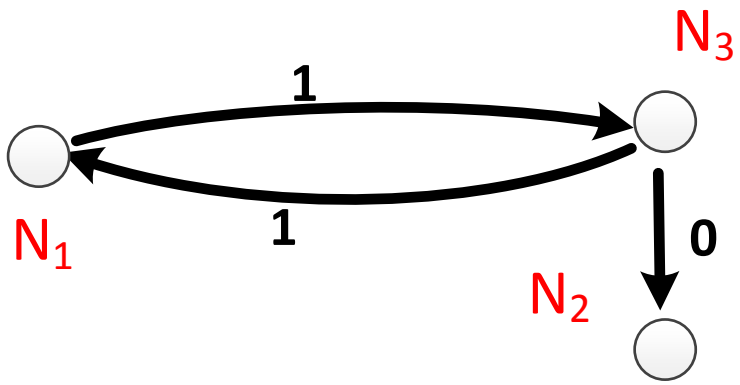


Figure 3.2 Node Link Diagram of Reduced DWM Graph of the Inverse-Widlar Circuit in Fig. 3.1(a)

3.3 Identification of the Positive Feedback Loops

After the Reduced DWM graph obtained, we can identify positive feedback loops easily from the definition of positive feedback loop. The reduced DWM Graph has one positive feedback loop and this loop is the sub-graph L_{PFL} defined by

$$L_{PFL} = (N_1, (N_1, N_3, 1), N_3, (N_3, N_1, 1), N_1)$$

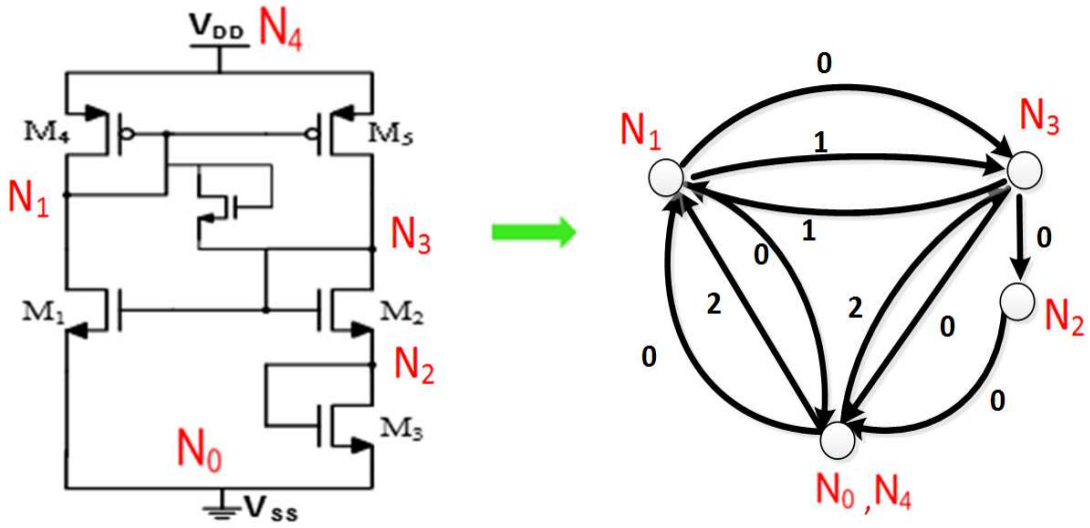
The positive feedback loop is highlighted in red in Fig. 3.3.

Figure 3.3 Positive Feedback Loop in Node Link Diagram of the Reduced DWM Graph

Since this circuit has a positive feedback loop, it is vulnerable to the presence of more than one stable equilibrium point. Whether this circuit actually has one or more undesired equilibrium points depends upon how the components in the circuit are sized. The remaining steps in the process can be used to determine if multiple equilibrium points actually exist.

3.4 Examples

In this part, an Inverse-Widlar structure with a start-up circuit will be presented. The purpose of this example is to illustrate that the start-up circuit would not break the positive feedback loop in the circuit. Also, it would not affect our algorithm to identify positive feedback loops.



(a) (b)

Figure 3.4 (a) An Inverse-Widlar Circuit with a Start-Up Circuit (b) Node Link Diagram of DWM Graph of an Inverse-Widlar Circuit with a Start-Up Circuit

The second step involves the creation of a reduced DWM Graph. The Node Link Diagram of reduced DWM Graph for the Inverse-Widlar circuit with a start-up circuit is depicted in Fig. 3.5.

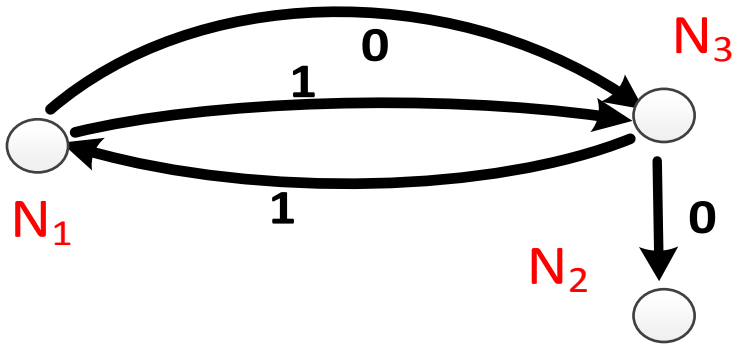


Figure 3.5 Node Link Diagram of Reduced DWM Graph of the Inverse-Widlar Circuit in Fig. 3.4(a)

After the Reduced DWM graph obtained, we can identify positive feedback loops easily from the definition of positive feedback loop. The reduced DWM Graph has one positive feedback loop and this loop is the sub-graph L_{PFL} defined by

$$L_{PFL} = (N_1, (N_1, N_3, 1), N_3, (N_3, N_1, 1), N_1)$$

The positive feedback loop is highlighted in red in Fig. 3.6.

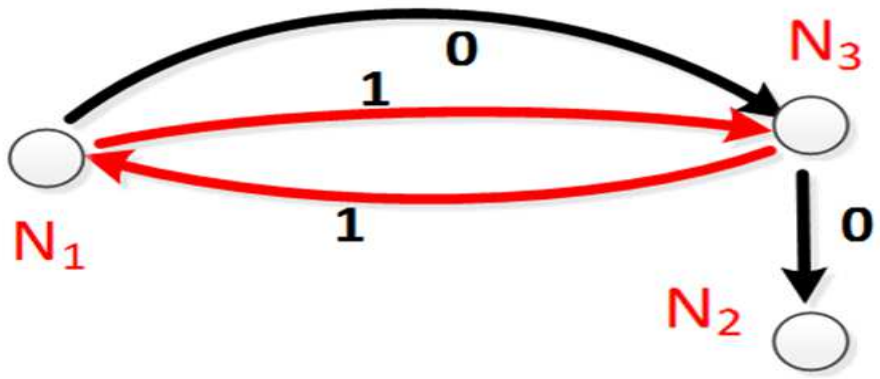


Figure 3.6 Positive Feedback Loop in Node Link Diagram of the Reduced DWM Graph

As can be seen from this example, the start-up circuit would not break the positive feedback loops in the circuit. As a result, this method works on circuits with start-up circuits and it provide a sufficient method to verify the effectiveness of start-up circuits in self-biasing circuits. Since this circuit has a positive feedback loop, it is vulnerable to the presence of more than one stable equilibrium point. Whether this circuit actually has one or more undesired equilibrium points depends upon how the components in the circuit are sized.

CHAPTER 4

IDENTIFYING MULTIPLE OPERATING POINTS

4.1 Breaking Positive Feedback Loops

In this section, we will focus on breaking positive feedback loops in reduced DWM graphs and the corresponding positive feedback loops in circuits. Consider the Node Link Diagram of reduced DWM graph of Inverse-Widlar circuit in Fig. 3.1(a) from last chapter as an example to demonstrate this process. The positive feedback loop can be broken at either node N_1 or N_3. Breaking the positive feedback loop at node N_3, two nodes are formed. N_3' and N_3'' where one branch in the positive feedback loop is connect to N_3' and another to N_3''. This breaking of the loop is depicted graphically in Fig. 4.1. This comprises Step 4 described in chapter 3.1.

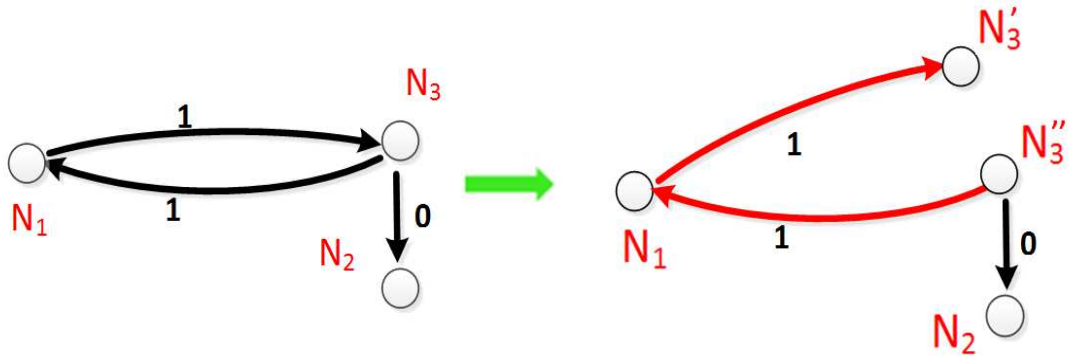


Figure 4.1 Breaking the Positive Feedback Loop in Node Link Diagram of Reduced DWM Graph

The corresponding breaking of the positive feedback loop in the circuit itself is shown in Fig. 4.2. This comprises Step 5 and step 6 is the homotopy analysis. The circuit is excited at node N_3''

with the voltage source V_x and terminated at node N_3' with the dependent current I_2. The current of the dependent current source is equal to the current flowing through voltage source V_x .

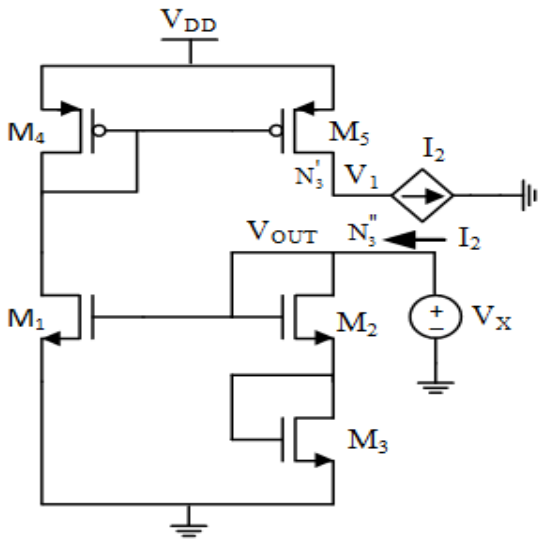


Figure 4.2 The New Inverse-Widlar Circuit

4.2 Creating Return Map using Homotopy Method

In this section, we focus on applying homotopy method to obtain return map and determine equilibrium points from return map. Consider the circuit from Fig. 4.2 as an example to demonstrate this process. The return map resulting from a homotopy sweep for a specific implementation of this circuit is shown in Fig. 4.3. Since this circuit has a single positive feedback loop, the intersection of the V_x=V_1 line with the return map will identify all operating points of the circuit. It can be seen that there are three intersection points. The uppermost intersection point is the desired DC operating point and one on the lower left is an undesired (Trojan) operating point. The middle intersection point is a quasi-stable operating point. Device sizes are shown in Table 4. We ran a DC sweep of Vx and this simulation is in TSMC 0.18um process with a 1.8V power supply.

Table 4.1 Device Sizes for New Inverse-Widlar Circuit

Transistor	Width(um)	Length(um)	Multiples
M1	0.3	0.9	1
M2	5	0.3	2
M3	7	0.3	2
M4	0.56	0.3	2
M5	0.5	0.72	6

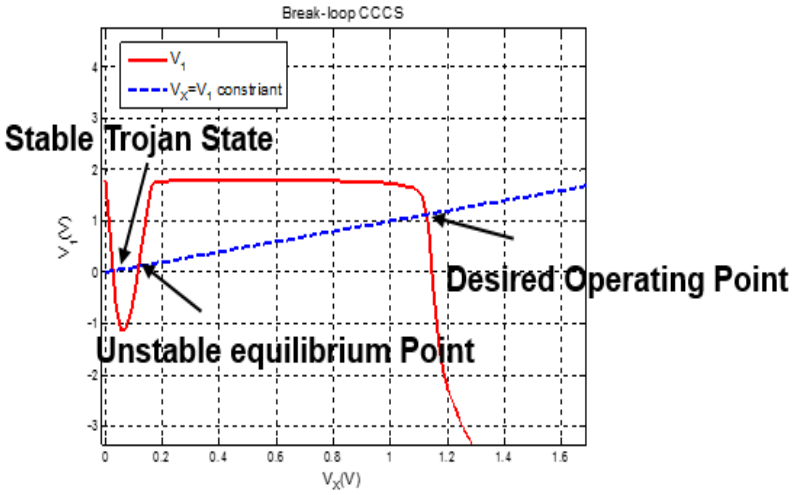


Figure 4.3 Return Map of the New Inverse-Widlar Circuit in Fig. 4.2

Though this example was based upon on a circuit with a single positive feedback loop, the method can be extended to circuits with two or more positive feedback loops but the computational complexity can become excessive in some circuits with more than two positive feedback loops.

CHAPTER 5

SUMMARY OF THE ALGORITHM

5.1 Summary

This algorithm has seven steps and this overall process can be summarized as follows:

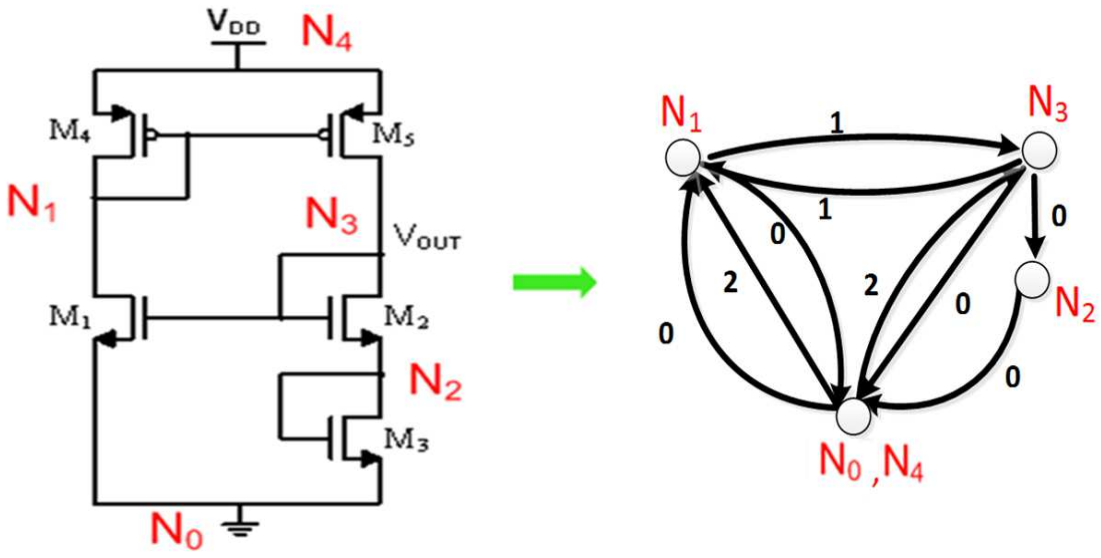
1. Create a DWM Graph of Circuit
2. Create a reduced DWM Graph
3. Identify positive feedback loops from the reduced DWM Graph
4. Break positive feedback loops in the reduced DWM Graph
5. Break corresponding positive feedback loops in the circuit
6. Apply homotopy method to obtain return map
7. Determine equilibrium points from return map

5.2 Examples

In this part, a summary of the algorithm will be presented. Two examples are used for illustrating this algorithm. The first example is an Inverse-Wildar circuit without a start-up circuit. Another example is an Inverse-Widlar circuit with a start-up circuit.

5.2.1 Inverse-Widlar Circuit without a Start-Up Circuit

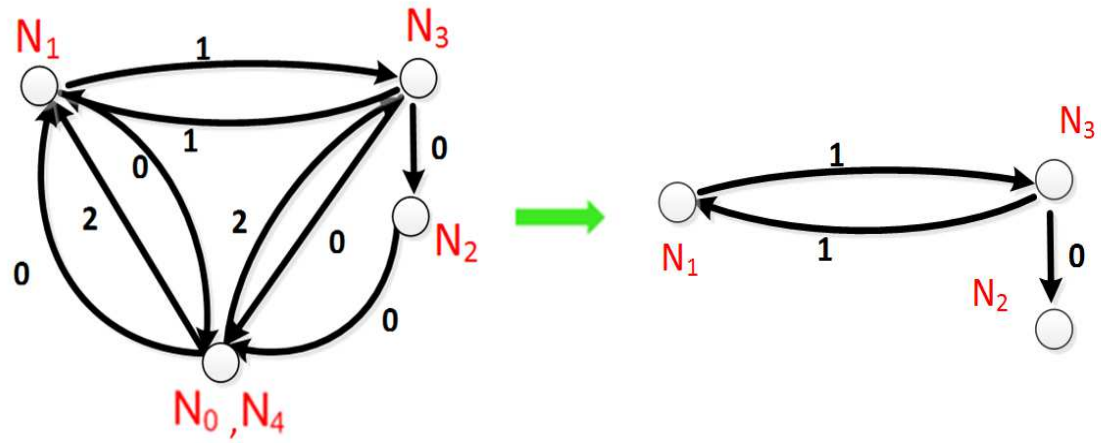
1. Create the DWM Graph of circuit by merging all Element, Directed, Weighted, Multi Graphs (EDWM Graph) into Directed, Weighted, Multi Graph (DWM Graph).



(a) (b)

Figure 5.1 (a) An Inverse-Widlar Circuit without a Start-Up Circuit (b) Node Link Diagram of DWM Graph of an Inverse-Widlar Circuit without a Start-Up Circuit

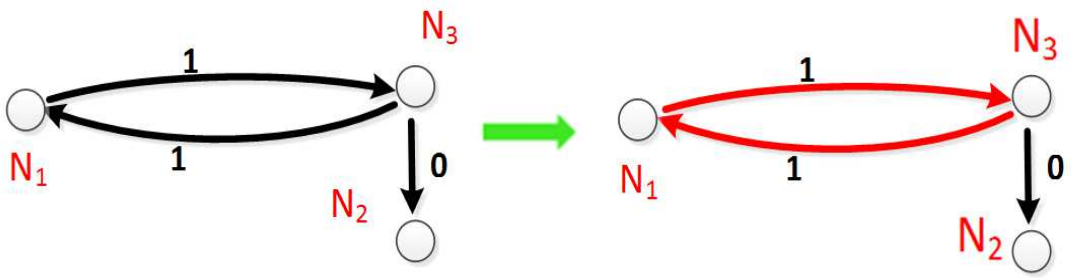
2. Create the reduced DWM Graph by eliminating Ground nodes and all branches connected to Ground nodes.



(a) (b)

Figure 5.2 (a) Node Link Diagram of DWM Graph of the Inverse-Wildar Circuit in Fig. 5.1(a) (b) Node Link Diagram of Reduced DWM Graph of the Inverse-Widlar Circuit in Fig. 5.1(a)

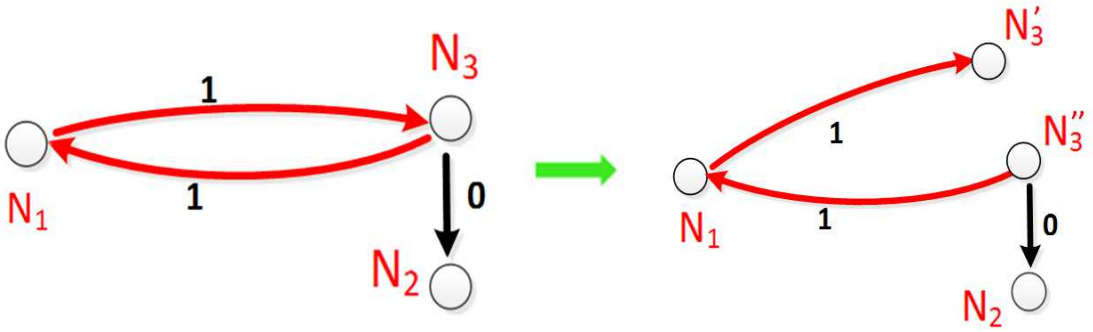
3. Identifying the positive feedback loops in reduced DWM Graph.



(a) (b)

Figure 5.3 (a) Node Link Diagram of reduced DWM Graph of the Inverse-Widlar Circuit in Fig. 5.1(a) (b) Positive Feedback Loop in Node Link Diagram of the Reduced DWM Graph

4. Breaking the positive feedback loop at node N_3, two nodes are formed. N_3' and N_3'' where one branch in the positive feedback loop is connect to N_3' and another to N_3''.



(a) (b)

Figure 5.4 (a) Positive Feedback Loop in Node Link Diagram of the Reduced DWM Graph (b) Breaking the Positive Feedback Loop in Node Link Diagram of Reduced DWM Graph

5. Breaking corresponding positive feedback loops in circuit. Create a new circuit by partitioning the corresponding node in original circuit into two nodes and exciting corresponding N_3'' with a

voltage source V_X and $N_3^{'}$ with dependent current source which current is equal to current flowing through the voltage source V_X .

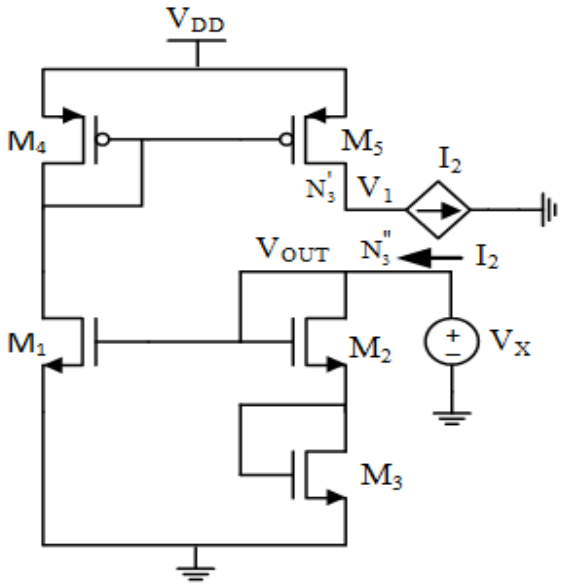


Figure 5.5 The New Inverse-Widlar Circuit

6. Apply homotopy method to obtain return map.

Claim: Intersection of $V_O = V_{in}$ line with return map will identify all operating points of the circuit.

Device sizes are shown on Table 5. We ran a DC sweep of Vx and this simulation is in TSMC 0.18um process with a 1.8 V power supply at 300K temperature.

Table 5.1 Device Sizes for New Inverse-Widlar Circuit

Transistor	Width(um)	Length(um)	Multiples
M1	0.3	0.9	1
M2	5	0.3	2
M3	7	0.3	2
M4	0.56	0.3	2
M5	0.5	0.72	6

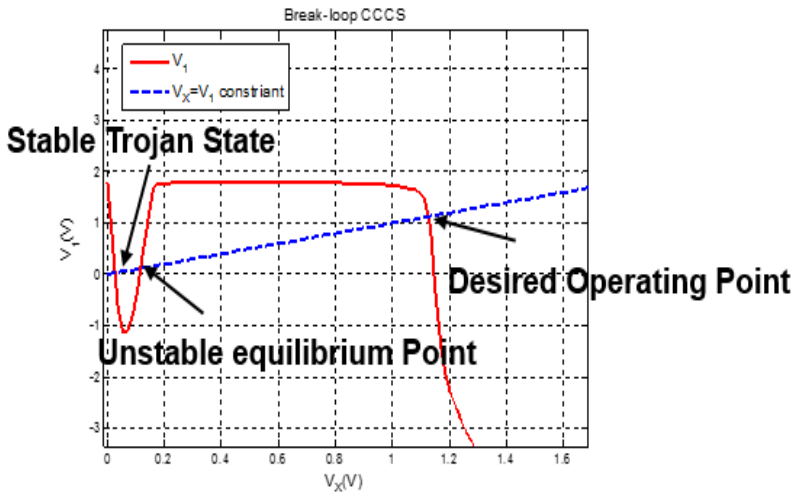
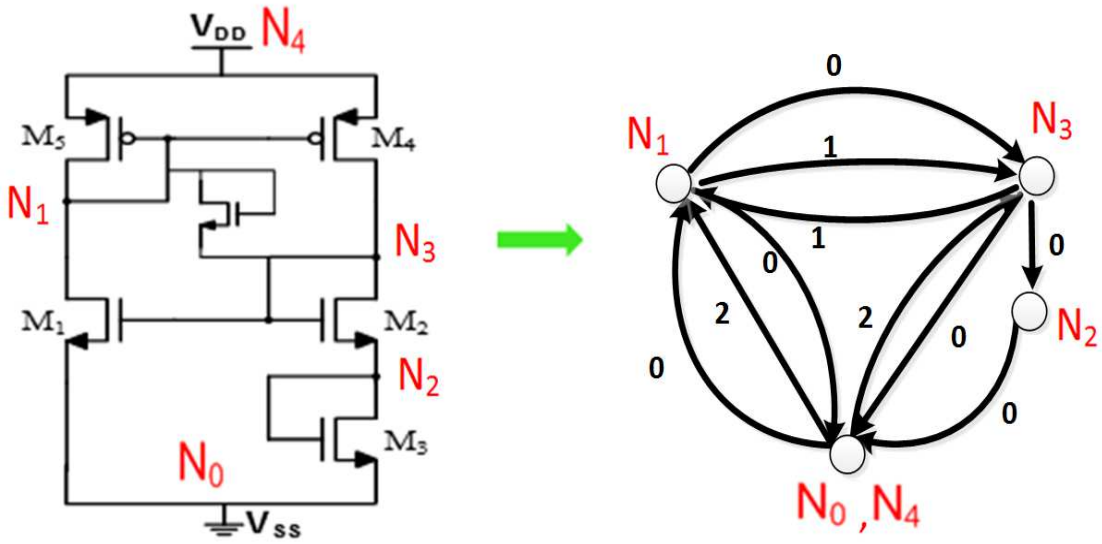


Figure 5.6 Return Map from Homotopy Sweep

It can be seen that there are three intersection points from the return map. The uppermost intersection point is the desired dc operating point and one on the lower left is an undesired (Trojan) operating point. The middle intersection point is a quasi-stable operating point. It indicates that this circuit has a Trojan State.

5.2.2 Inverse-Widlar Circuit with a Start-Up Circuit

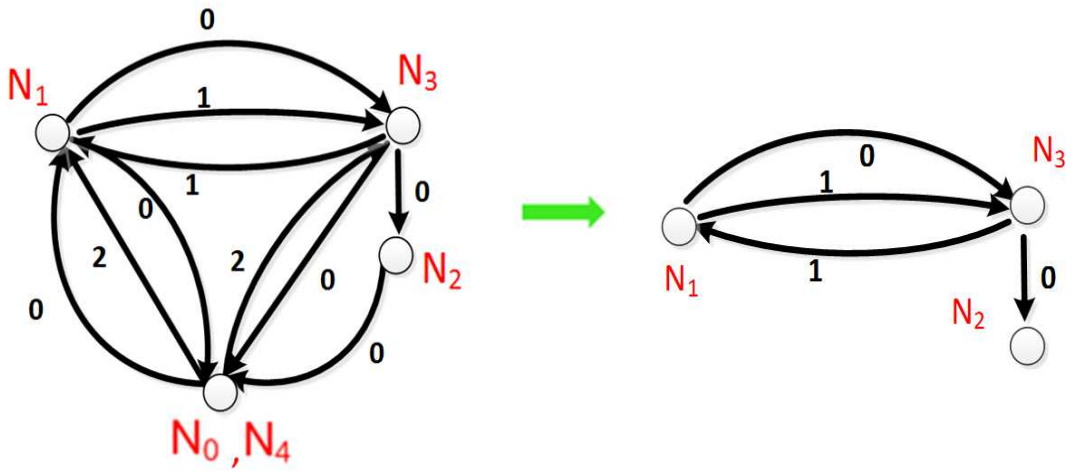
1. Create the DWM Graph of circuit by merging all Element, Directed, Weighted, Multi Graphs (EDWM Graph) into Directed, Weighted, Multi Graph (DWM Graph).



(a) (b)

Figure 5.7 (a) An Inverse-Widlar Circuit with a Start-Up Circuit (b) Node Link Diagram of DWM Graph of an Inverse-Widlar Circuit with a Start-Up Circuit

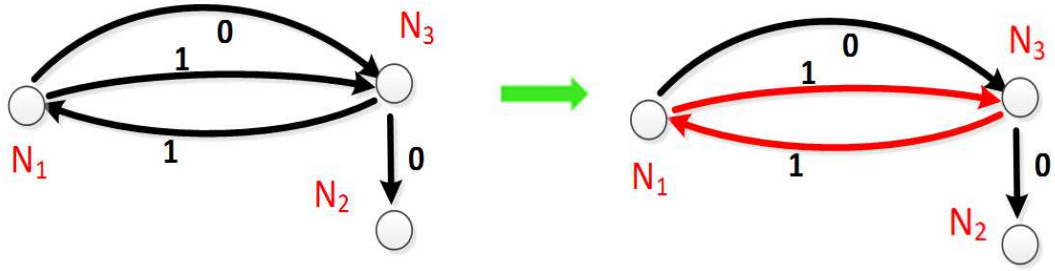
2. Create the reduced DWM Graph by eliminating Ground nodes and all branches connected to Ground nodes.



(a) (b)

Figure 5.8 (a) Node Link Diagram of DWM Graph of the Inverse-Wildar Circuit in Fig. 5.7(a) (b) Node Link Diagram of Reduced DWM Graph of the Inverse-Widlar Circuit in Fig. 5.7(a)

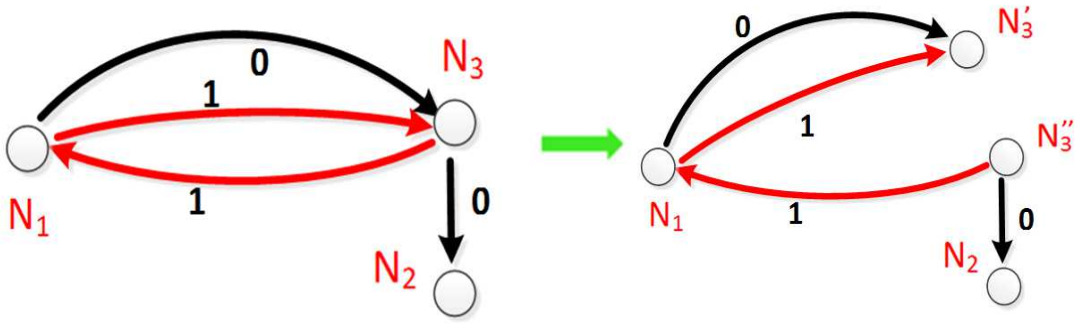
3. Identifying the positive feedback loops in reduced DWM Graph.



(a) (b)

Figure 5.9 (a) Node Link Diagram of DWM Graph of the Inverse-Widlar Circuit in Fig. 5.7(a) (b) Positive Feedback Loop in Node Link Diagram of the Reduced DWM Graph

4. Breaking the positive feedback loop at node N_3, two nodes are formed. N_3' and N_3'' where one branch in the positive feedback loop is connect to N_3' and another to N_3''.



(a) (b)

Figure 5.10 (a) Positive Feedback Loop in Node Link Diagram of the Reduced DWM Graph (b) Breaking the Positive Feedback Loop in Node Link Diagram of Reduced DWM Graph

5. Breaking corresponding positive feedback loops in circuit. Create a new circuit by partitioning the corresponding node in original circuit into two nodes and exciting corresponding N_3'' with a voltage source V_X and N_3' with dependent current source which current is equal to current flowing through voltage source V_X.

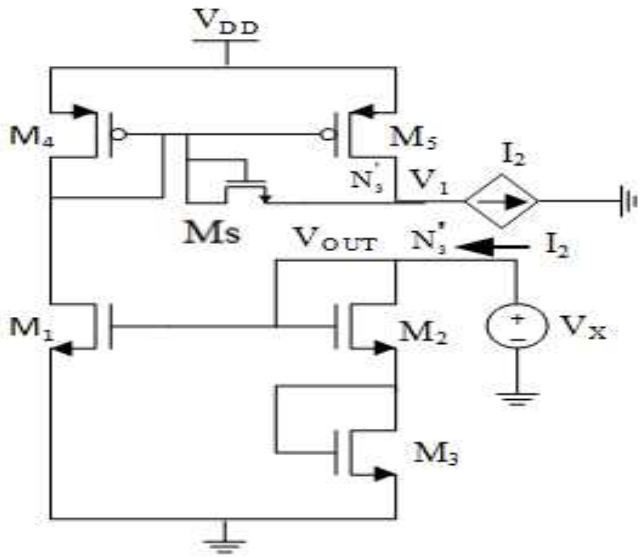


Figure 5.11 The New Inverse-Widlar Circuit with a Start-Up Circuit

6. Apply homotopy method to obtain return map.

Claim: Intersection of $V_O = V_{in}$ line with return map will identify all operating points of the circuit.

Device sizes are shown in Table 6. We ran a DC sweep of Vx and this simulation is in TSMC 0.18um process with a 1.8 V power supply.

Table 5.2 Device Sizes for New Inverse-Widlar Circuit

Transistor	Width(um)	Length(um)	Multiples
M1	0.3	0.9	1
M2	5	0.3	2
M3	7	0.3	2
M4	0.56	0.3	2
M5	0.5	0.72	6
Ms	0.5	0.72	6

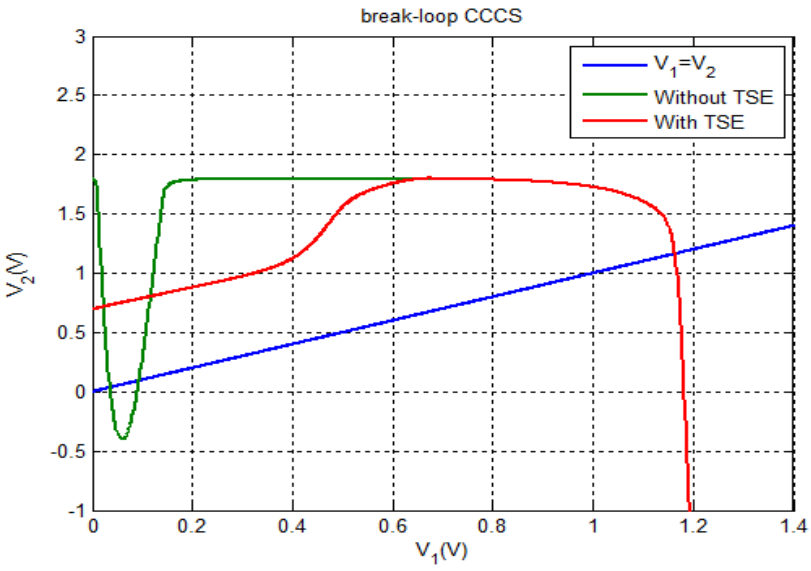


Figure 5.12 Return Map from Homotopy Sweep

Compare the return map with Inverse-Widlar circuit without a start-up circuit. We can find that this circuit has no Trojan State since it only has one intersection point between $V_O = V_{in}$ line and the return map.

CHAPTER 6

THERMAL NOISE IN SAMPLE-AND-HOLD CIRCUITS

6.1 Problem Statement

Sample-and-Hold circuits are wildly used in mixed-signal circuits such as data converters, filters etc. Thermal noise is often a design limitation in mixed-signal designs. Many literatures and analog textbooks state that the thermal noise voltage sampled on a capacitor is $\sqrt{k\,T\ /\ C}$ where k is Boltzmann constant, T is temperature and C is capacitance [21][24].

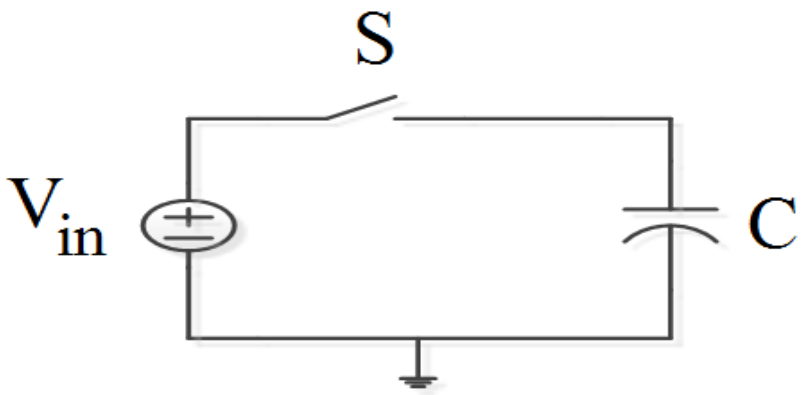


Figure 6.1 A Sample-and-Hold Circuit

From the expression of thermal noise voltage, we can find that thermal noise is highly related to the capacitor value and independent of the resistor. The only way to reduce thermal noise voltage is to increase the capacitance. However, a large capacitor increases the settling time and reduce the sampling rate. Meanwhile, layout area and power dissipation will be increased. No literatures introduce a method for reducing thermal noise without increasing capacitance. Making the thermal noise voltage sampled on capacitor independent of capacitor may give designer opportunities for improving system performance and more freedom to design circuits.

In this chapter, a method for reducing thermal noise voltage sampled on a sampling capacitor below $\sqrt{kT/C}$ is introduced.

6.2 Approach

Continuous-time domain thermal noise on RC circuit:

$$\overline{v_{out}^2} = 4kTR\int_0^\infty \left|\frac{1}{1+j2\pi RCf}\right|^2 df \quad (1)$$

$$= 4kTR\times\frac{\pi}{2}\times\frac{1}{2\pi RC} \quad (2)$$

$$= \frac{kT}{C} \quad (3)$$

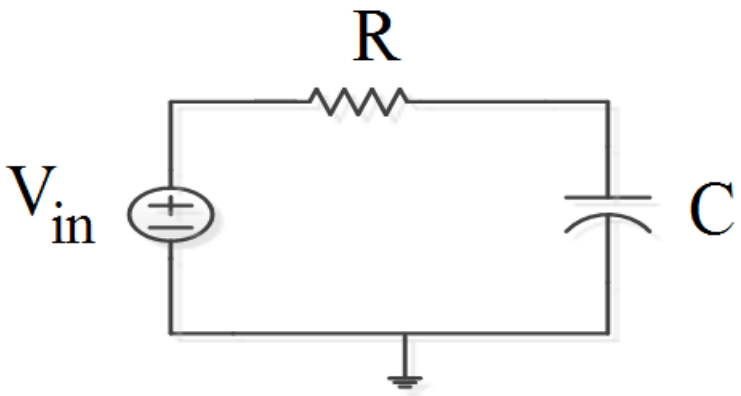


Figure 6.2 A First-Order RC Circuit

For sample-and-hold circuit in Fig. 6.1, thermal noise voltage sampled on C is the same as the first-order RC circuit in Fig. 6.2. The thermal noise sampled on C is $\sqrt{kT/C}$. Our idea is to use a sampled buffer to limit the noise bandwidth so that the overall thermal noise voltage sampled on sampling capacitor will be reduced since the noise bandwidth is smaller. At the same

time, a smaller sampling capacitor can be used since the noise bandwidth is independent of sampling capacitor. The schematic for this sampled buffer is shown in Fig. 6.3.

6.2.1 Bandwidth of Operational-Amplifier

Consider a sampled buffer in Fig. 6.3. Assume the op-amp is two-stage and well-compensated.

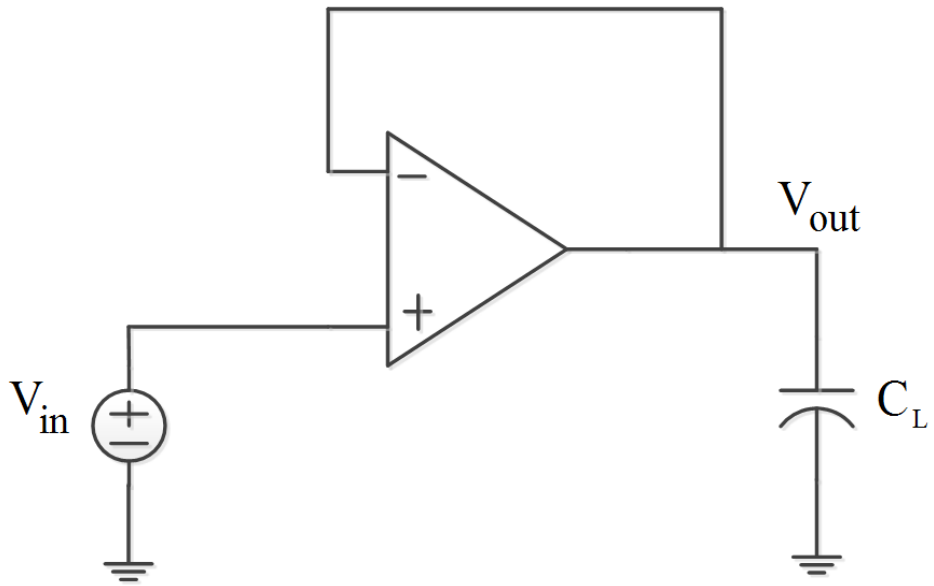


Figure 6.3 A Sampled Buffer

Since the op-amp is under negative feedback, the closed-loop bandwidth can be calculated as:

$$BW_{CL} = (1 + A\beta)\,\mathrm{BW}_{OL}$$
$$A = gm_1 \times R_{out1} \times gm_2 \times R_{out2}$$

where

BW_{CL} closed-loop bandwidth;

W_{OL} open-loop bandwidth;

A open-loop gain;

β feedback factor.

Open-loop bandwidth can be obtained by:

$$BW_{OL} = \frac{1}{R_{out1} \times (1 + gm_2 \times R_{out2}) Cc}$$

Cc is compensation capacitor.

After obtained open-loop bandwidth, the closed-loop bandwidth is:

$$BW_{CL} = (1 + A\beta)\,\mathrm{BW}_{OL}$$

$$(1 + gm_1 \times R_{out1} \times gm_2 \times R_{out2}) \frac{1}{R_{out1} \times (1 + gm_2 \times R_{out2}) Cc}$$

$$\approx \frac{gm_1 \times R_{out1} \times gm_2 \times R_{out2}}{R_{out1} \times gm_2 \times R_{out2} \times Cc}$$

$$\approx \frac{gm_1}{Cc}$$

From closed-loop bandwidth expression, we can find that the closed-loop bandwidth is independent of output capacitor but highly related to the compensation capacitor and transconductance of input pair.

6.2.2 AC Simulation Result

Since the closed-loop bandwidth of sampled buffer is not dependent on output capacitor if this Op-Amp is well-compensated. We can use this sampled buffer to make thermal noise voltage sampled on sampling capacitor less than $\sqrt{k\,T\ /\ C}$. Although noise from Op-Amp would bring more noise to output, we can use some design techniques to minimize the noise from Op-Amp. The schematic of Op-Amp is shown in Fig. 6.4 and device sizes are summarized

in Table 7. The schematic of sampled buffer with sampling capacitor is shown in Fig. 6.3. C_L is the sampling capacitor. We ran an AC noise simulation and this simulation is in AMI0.6 process with a 5V power supply at 300K temperature.

Table 6.1 Device Sizes for Op-Amp

Transistor	Width(um)	Length(um)	Multiples
M_1	6	1.2	3000
M_2	6	1.2	3000
M_3	3	4.5	4
M_4	3	4.5	4
M_5	1.5	0.6	100
M_6	3	4.5	16
M_7	6	1.2	6
M_8	1.5	0.6	100
M_9	6	1.2	12
M_{10}	6	1.2	6
M_{11}	3	4.5	16
M_C	6	0.6	10
M_n	6	0.6	10
M_p	6	0.6	10

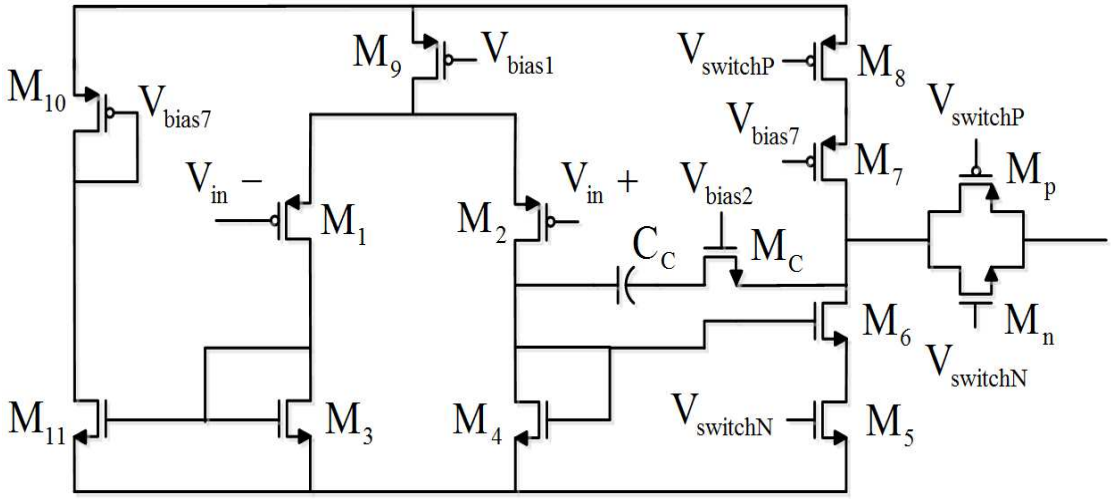


Figure 6.4 Schematic of Op-Amp

The accumulated thermal noise voltage on sampling capacitor C_L is shown in Fig. 6.5. The x-axis represents the stop frequency for integration of thermal noise voltage. From Fig. 6.5, the thermal noise voltage is saturated at approximately 60uV which means that the maximum thermal noise voltage sampled on C_L is 60uV.

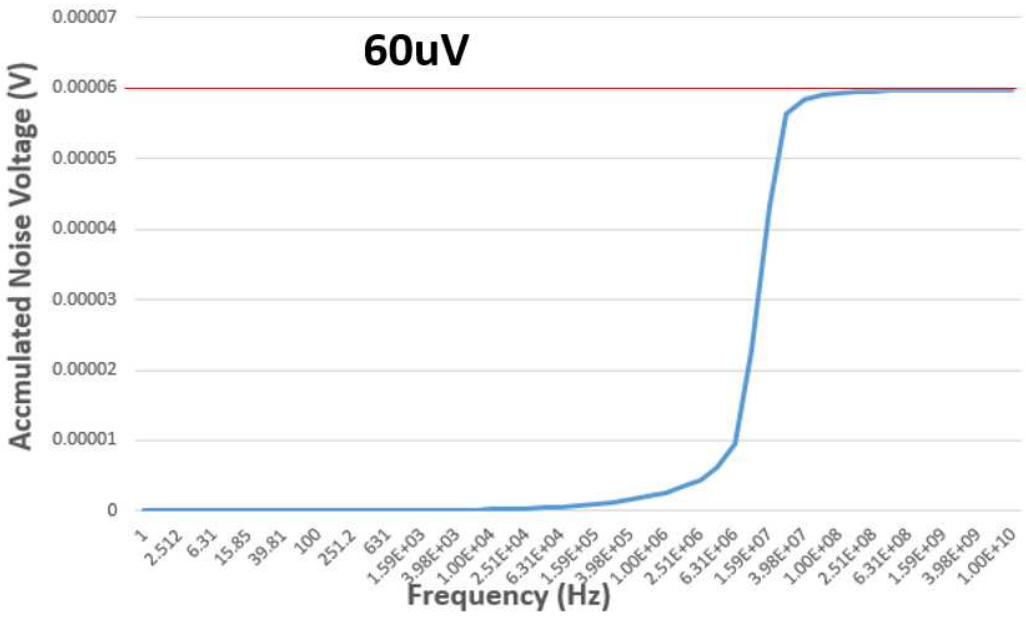


Figure 6.5 Simulation Results of Accumulated Noise Voltage

For the first-order RC circuit in Fig. 6.2, output capacitor is 100fF. Output noise voltage at 300K temperature is:

$$V_n = \sqrt{\frac{kT}{C}} = \sqrt{\frac{1.38\times10^{-23}\times300}{100\times10^{-15}}}$$
$$= 203.47uV$$

Compare this noise with the noise of sampled buffer in Fig. 6.5,

$$\frac{60uV}{203.47uV} \approx \frac{1}{3.4}$$

This noise is approximately 3.4 times smaller than the first-order RC circuits. Output noise voltage is reduced dramatically with the same output capacitor.

6.2.3 Discrete-Time Domain Noise

The continuous-time domain noise can be obtained from simulation. How can the sampling process be analyzed or simulated? Steady-State noise analysis is not applicable. For this problem, transient noise model is used. The RMS noise voltage can be obtained:

$$\overline{v_{rms}} = \sqrt{\frac{1}{N}\sum_{k=1}^{N} v^2(\mathrm{kT})}$$

We ran transient simulation to obtain the discrete-time domain noise for the same circuit in Fig. 6.3. This simulation is in AMI0.6 process with a 5V power supply at 300K temperature. 25 samples are took and shown in Table 8.

Table 6.2 25 Noise Samples from the Sampled Buffer

Samples	Voltage(V)	Samples	Voltage(V)
1	1.364014595	14	1.364207997
2	1.364027821	15	1.364134977
3	1.364011807	16	1.364090158
4	1.364063346	17	1.364083964
5	1.364056483	18	1.364095229
6	1.364072126	19	1.363974012
7	1.364119004	20	1.364086905
8	1.364036319	21	1.364065862
9	1.364051634	22	1.364022091
10	1.364064461	23	1.364199076
11	1.364028666	24	1.36412531
12	1.364197579	25	1.364176656
13	1.364130844		

$$V_{n,rms} = \sqrt{\frac{\sum_{i=1}^{25}(a_i - \overline{A})^2}{25}}$$
$$= 61.799uV$$

In this equation, $\overline{A}$ is the average value of sampled noise outputs and a_i is the individual sampled noise voltage. Compare the noise from sampled buffer with first-order RC circuit,

$$\frac{61.799uV}{203.47uV} = \frac{1}{3.36}$$

Noise on C is about 3.36 times smaller than the first-order RC circuit.

6.3 Applications

In this part, we are going to apply our noise reduction technique to some practical applications. Take the switched-capacitor circuit in Fig. 6.6 as an example. The capacitance of Capacitor C_1 and C_2 are 100fF. S_1, S_2, S_3, S_4 and S_5 are transmission gate. More detail about this switched-capacitor circuit is shown in Fig. 6.7. Device sizes for this circuit are shown in Table 9.

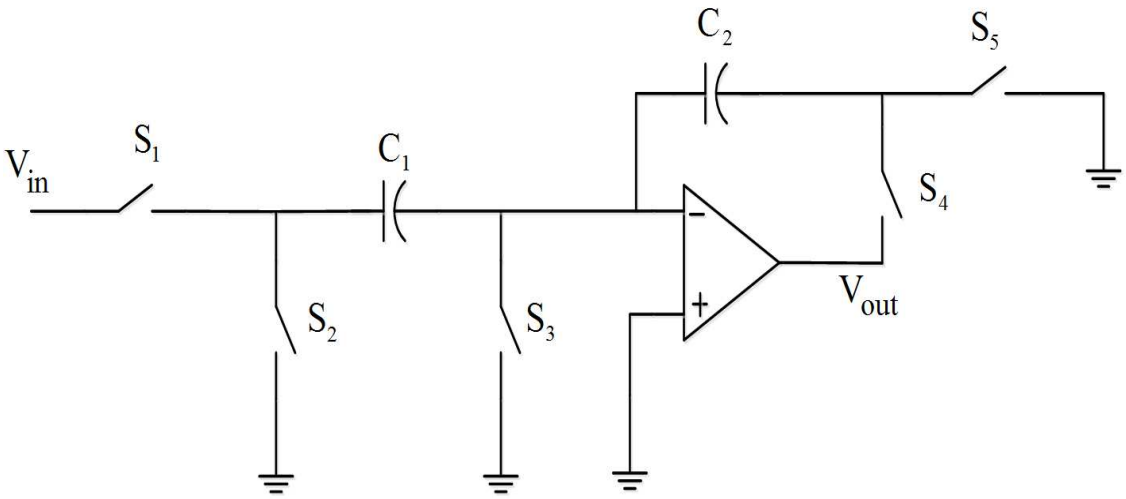


Figure 6.6 A Switched-Capacitor Circuit

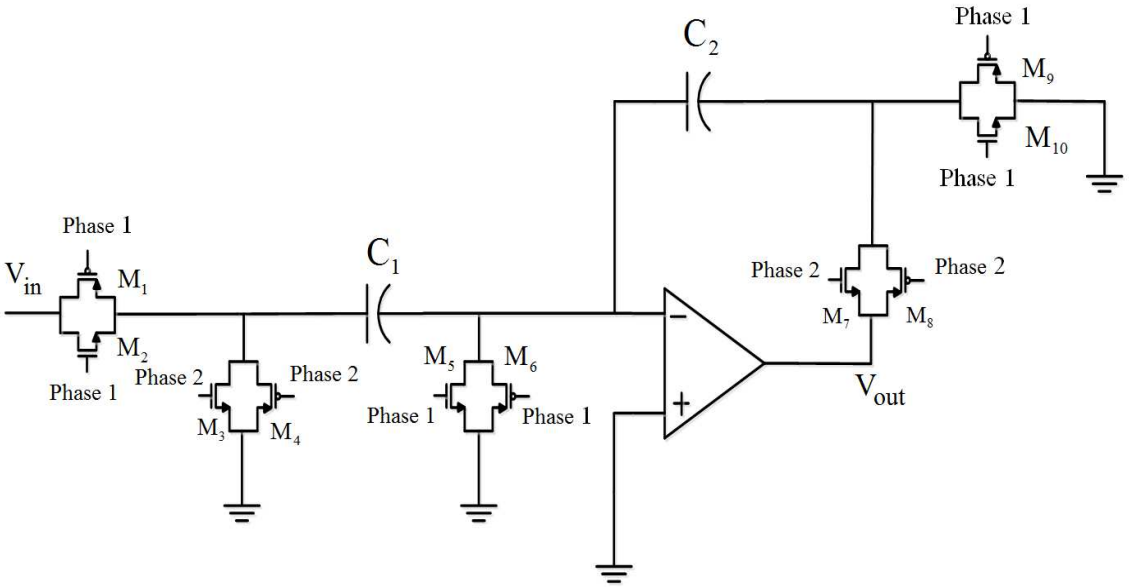


Figure 6.7 The Equivalent Switched-Capacitor Circuit of Fig. 6.6

Table 6.3 Transistor Sizes for Switches

Transistor	Width(um)	Length(um)	Multiples
M_1	6	0.6	120
M_2	6	0.6	120
M_3	6	0.6	120
M_4	6	0.6	120
M_5	6	0.6	10
M_6	6	0.6	10
M_7	6	0.6	1200
M_8	6	0.6	1200
M_9	6	0.6	120
M_{10}	6	0.6	120

The hand calculation for the overall thermal noise voltage at output is calculated as,

Phase 1:

In phase 1, switches S_1, S_3 and S_5 are on. The circuit is shown in Fig. 6.8.

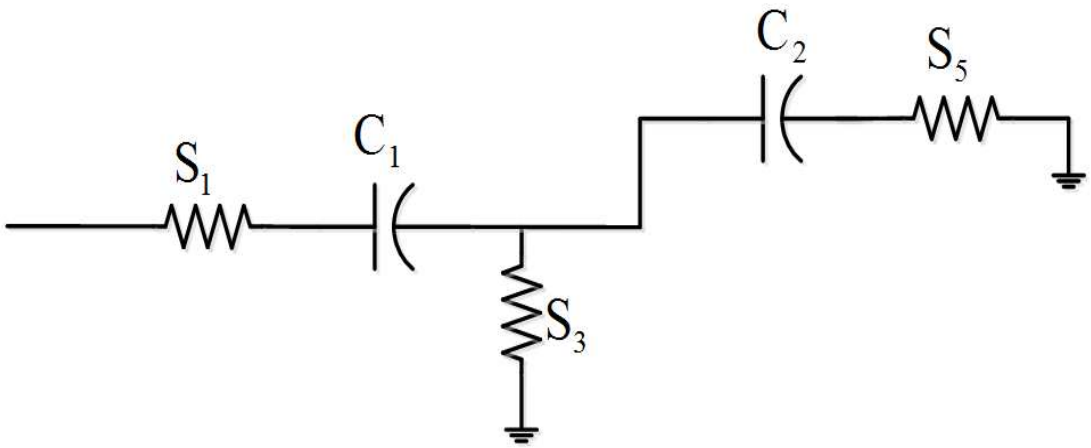


Figure 6.8 The Switched-Capacitor Circuit in Phase 1

Each switch has an on-resistance so that there is a sampled thermal noise voltage on each capacitor caused by these switches.

Thermal Noise on C_1

$$\overline{V_{c1}^2} = \int_0^\infty 4kTR_{on}\left|\frac{1}{1+j2\pi fR_{on}C_1}\right|^2 df$$

$$= \frac{kT}{C_1}$$

Thermal Noise on C_2

$$\overline{V_{c2}^2} = \int_0^\infty 4kTR_{on}\left|\frac{1}{1+j2\pi fR_{on}C_2}\right|^2 df$$
$$= \frac{kT}{C_2}$$

Phase 2:

In phase 2, switches S_2 and S_4 are on. The circuit is shown in Fig. 6.9.

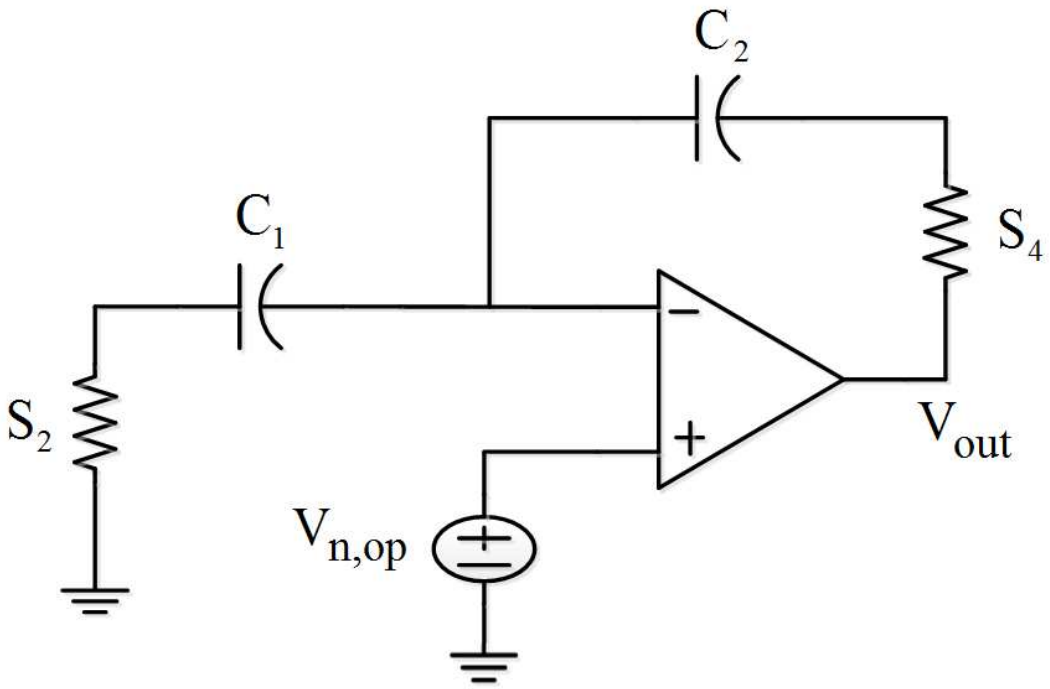


Figure 6.9 The Switched-Capacitor Circuit in Phase 2

There are four noise sources, thermal noise from S_2, S_4, Op-Amp and noise sampled on C_1 and C_2 from Phase 1.

Thermal Noise from S_2

The closed-loop bandwidth of Op-Amp is calculated as,

$$BW = \frac{\beta g_{m1}}{C_0}$$

The thermal noise from S_2 at output is,

$$\overline{V_{n,S2}^2} = \int_0^\infty 4kTR_{on2}\left(\frac{C_1}{C_2}\right)^2 \left|\frac{1}{1+\frac{j2\pi f}{BW}}\right|^2 df$$

$$= R_{on2}\beta g_{m1}\left(\frac{C_1}{C_2}\right)^2 \frac{kT}{C_0}$$

In this equation, C_0 is the compensation capacitor of Op-Amp.

Thermal Noise from Operational-Amplifier

Assume the transconductance of input pair of op-amp is very large, Power spectral density of Op-Amp is

$$PSD \approx \frac{16kT\alpha}{3g_{m1}}$$

In this equation, α is the noise constant of transistor.

The thermal noise from Op-Amp at output is,

$$\overline{V_{n,op}^2} = \int_0^\infty \frac{16kT\alpha}{3g_{m1}}\left(1+\frac{C_1}{C_2}\right)^2 \left|\frac{1}{1+\frac{j2\pi f}{BW}}\right|^2 df$$

$$= \frac{4kT\alpha}{3\beta C_0}$$

Thermal Noise from S_4

The thermal noise from S_4 at output is,

$$\overline{V_{n,S4}^2} = \int_0^\infty 4kTR_{on4}\left|\frac{1}{1+\frac{j2\pi f}{BW}}\right|^2 df$$

$$= \frac{kTR_{on4}\beta g_{m1}}{C_0}$$

Thermal Noise Sampled on C_1 and C_2 from Phase 1

For C_1, all thermal noise voltages are transferred to C_2. As a result, the thermal noise voltage from C_1 at output is,

$$\overline{V_{n,c1}^2} = \frac{kTC_1}{C_2^2}$$

For C_2, thermal noise voltage from C_2 at output is,

$$\overline{V_{n,c2}^2} = \frac{kT}{C_2}$$

The overall thermal noise voltage at output from all phases is calculated as,

$$\overline{V_{out}^2} = \frac{kTC_1}{C_2^2} + \frac{kT}{C_2} + \frac{kTR_{on4}\beta g_{m1}}{C_0} + \frac{4kT\alpha}{3\beta C_0} + R_{on2}\beta g_{m1}\left(\frac{C_1}{C_2}\right)^2 \frac{kT}{C_0}$$

Since C_1 and C_2 are equal in our case, the equation can be simplified as,

$$\overline{V_{out}^2} = 2\frac{kT}{C_1} + \frac{kTR_{on4}\beta g_{m1}}{C_0} + \frac{4kT\alpha}{3\beta C_0} + R_{on2}\beta g_{m1}\frac{kT}{C_0}$$

Assume C_0 is very large. Output thermal noise voltage can be reduced to,

$$\overline{V_{out}^2} = 2\frac{kT}{C_1}$$

$$\Rightarrow \overline{V_{out,\mathrm{rms}}} = \sqrt{\frac{2kT}{C_1}}$$

$$= \sqrt{\frac{2\times 1.38\times 10^{-23}\times 300}{100\times 10^{-15}}}$$

$$= 287.75uV$$

We ran transient simulation to obtain discrete-time domain noise and this simulation is in AMI06 process with a 5V power supply at 300K temperature. Our simulation result is corresponding to our hand calculation. Simulated sampled noise voltage at V_{out} is approximately 300uV.

From the hand calculation, we found that the major noise contribution is from thermal noise sampled on capacitor C_1 and C_2 in phase 1. As a result, we apply our noise reduction technique to switches S_1 and S_5. The noise compensated switched-capacitor circuit is shown in Fig. 6.10.

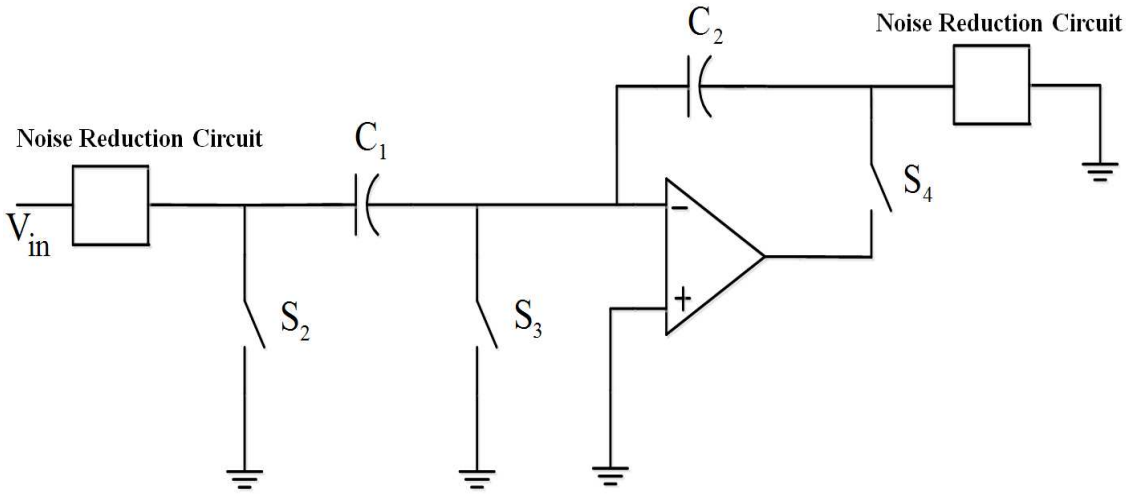


Figure 6.10 The Switched-Capacitor Circuit with Noise Reduction Circuits

The simulation result is shown in Table 10 and this simulation is in AMI06 process with a 5V power supply at 300K temperature. 25 samples are taken in the transient simulation.

Table 6.4 25 Noise Samples at Output from Switched-Capacitor Circuit

Samples	Voltage (V)	Samples	Voltage (V)
1	1.8274461322	14	1.8275665887
2	1.8276563096	15	1.8272900321
3	1.8275505077	16	1.8276122205
4	1.8274983450	17	1.8274132304
5	1.8273434897	18	1.8273429124
6	1.8274149350	19	1.8272439624
7	1.8273325093	20	1.8274898670
8	1.8274114451	21	1.8274797170
9	1.8274535567	22	1.8273336398
10	1.8274762349	23	1.8274145198
11	1.8273972757	24	1.8275112729
12	1.8271931230	25	1.8276096166
13	1.8272482298		

$$V_{n,rms} = \sqrt{\frac{\sum_{i=1}^{25}(a_i - \overline{A})^2}{25}}$$
$$= 118.237uV$$

In this equation, $\overline{A}$ is the average value of sampled outputs and a_i is the individual sampled noise voltage.

Without Noise Reduction Circuits, the simulated noise voltage at output is,

$$V_{n,rms} = 299.68uV$$

With the Noise Reduction Circuit, the simulated noise voltage at output is,

$$V_{n,rms} = 118.237uV$$

Compare these two values, the overall noise voltage at output can be reduced by approximately a factor of three. Using this technique, designers can use small sampling capacitors but have decent noise performance.

6.4 Summary

In this section, we proved a concept that thermal noise voltage sampled on capacitor can be reduced below $\sqrt{k\,T\ /\ C}$. Meanwhile, we showed an example how to apply our technique to some practical circuits to reduce the overall thermal noise. Using this technique, designers can have more freedom to design circuits and improve the noise performance.

Chapter 7

THERMAL NOISE IN CAPACITOR DAC OF SAR ADC

7.1 Introduction

In high resolution SAR ADC designs, many papers state that the minimum capacitance of capacitor DAC is determined by the thermal noise limitation. This thermal noise limitation is kT/C where k is Boltzmann constant, T is temperature and C is the total capacitance of capacitor DAC. Moreover, they assume this is the input-referred noise for the whole ADC. However, this calculation ignores the noises from charge-redistribution mode completely. Meanwhile, no literatures introduce any method about numerical calculation of thermal noise from charge-redistribution mode in capacitor DAC. In this chapter, a numerical calculation of thermal noise from charge-redistribution mode of SAR ADC is introduced.

7.2 Analysis and Calculation of Thermal Noise

Consider Fig. 7.1 as an example. This is a 3-bits SAR ADC in hold mode. In hold mode, there is a thermal noise voltage from sample mode stored on each capacitor.

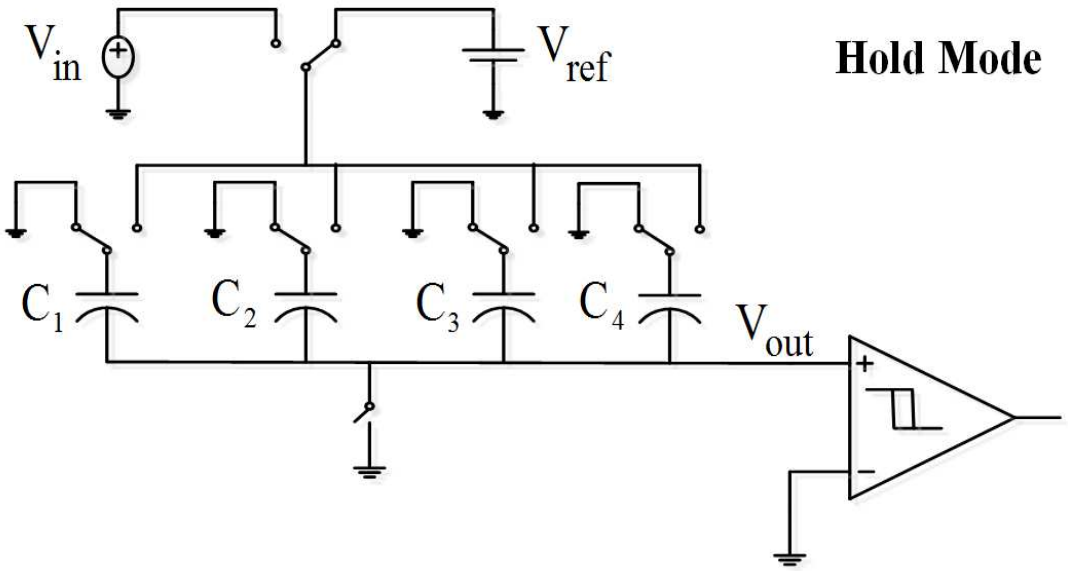


Figure 7.1 SAR ADC in Hold Mode

This noise voltage can be calculated as:

$$v_{i,rms} = \sqrt{\frac{kT}{C_i}}$$

$$i = 1, 2, 3, 4$$

After sample-and-hold mode, SAR ADC goes into charge-redistribution mode. Consider MSB conversion as an example. Fig. 7.2 shows the capacitor DAC of SAR ADC in charge-redistribution mode.

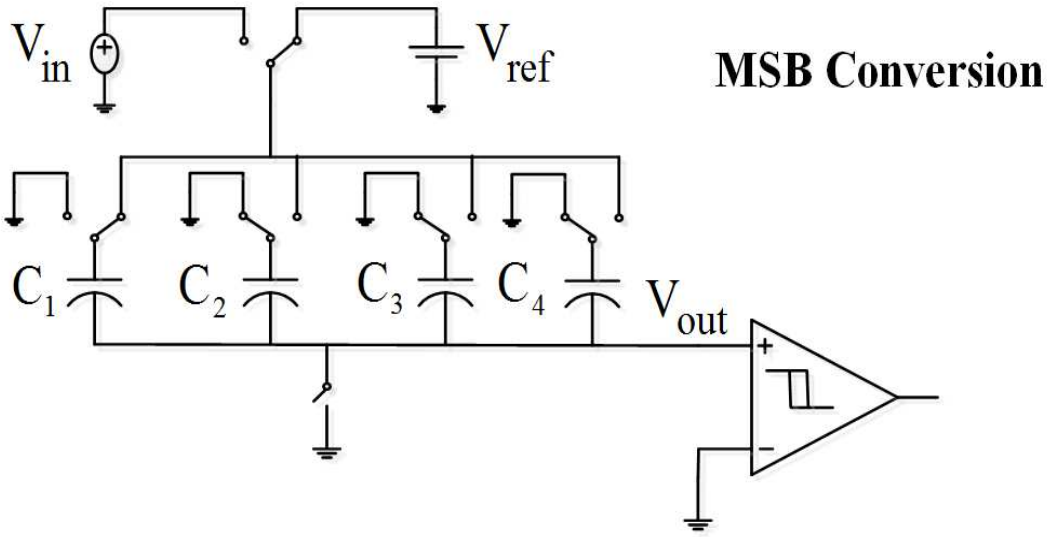


Figure 7.2 Capacitor DAC of SAR ADC in Charge-Redistribution Mode

The equivalent circuit of Fig. 7.2 is shown in Fig. 7.3. In MSB conversion, capacitor $C_{t1}$is equal to capacitor C_{t2}.

$$C_{t1} = C_1$$
$$C_{t2} = C_2 + C_3 + C_4$$

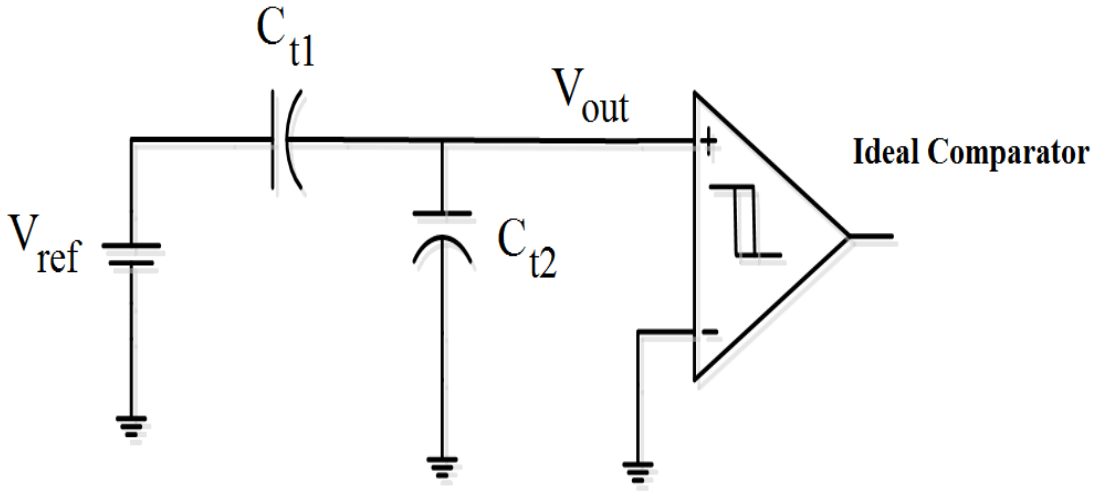


Figure 7.3 Equivalent Circuit of MSB Conversion

Fig. 7.4 shows the equivalent circuit with noise sources of Fig. 7.3. There is a sampled thermal noise voltage on C_{t1} which is V_{n1} and sampled thermal noise voltage on C_{t2} which is V_{n2}. Also, there are continuous-time noise sources V_{n3} and V_{n4} from switches. At this point, noise from comparator is not included in our analysis since we are analyzing noise from capacitor DAC. Assume comparator is ideal.

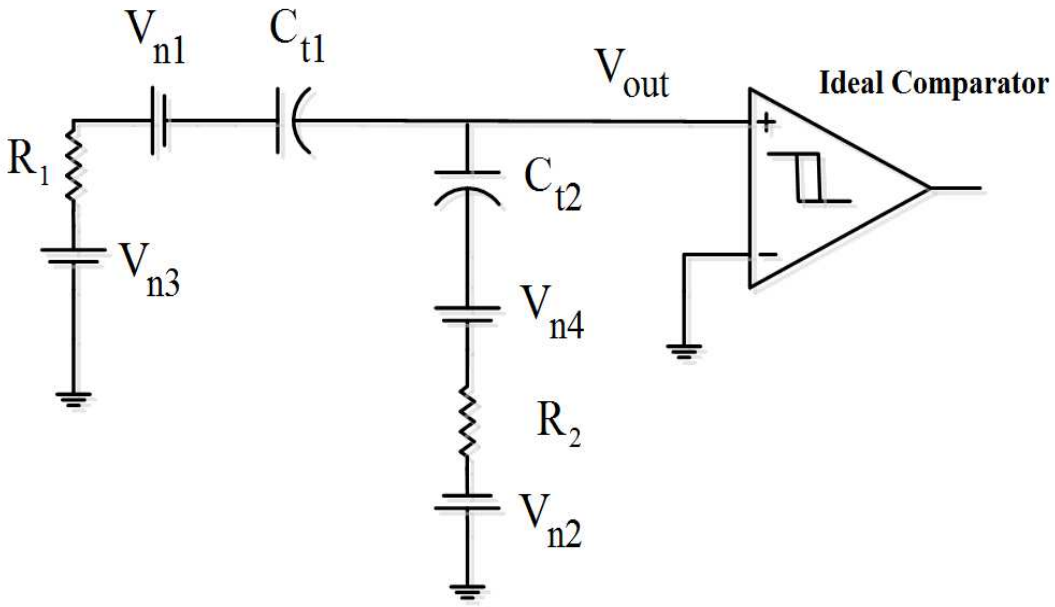


Figure 7.4 The Equivalent Circuit with Noise Sources of MSB Conversion

There are four noise sources and we use superposition to analyze this circuit. In the first place, V_{n1} is the only noise source we consider. Assume V_{c1} is the noise voltage across capacitor C_{t1} and V_{c2} is the noise voltage across C_{t2}. The equivalent circuit for noise source V_{n1} is shown in Fig. 7.5.

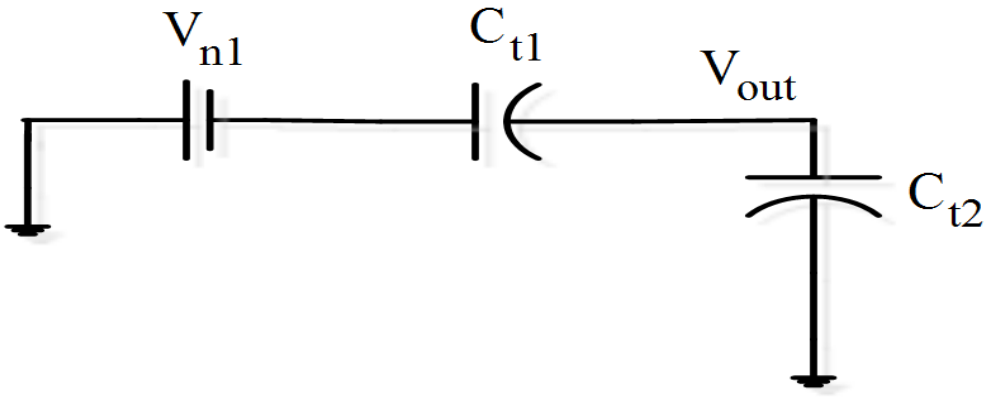


Figure 7.5 The Equivalent Circuit for Noise Source V_{n1}

$$V_{c1} = (-V_{n1}) \times (\frac{C_{t2}}{C_{t1} + C_{t2}})$$

$$V_{c2} = (-V_{n1}) \times (\frac{C_{t1}}{C_{t1} + C_{t2}})$$

V_{c1}, V_{c2} and V_{n1} are correlated. Add them together,

$$V_{tot1} = V_{c1} + V_{c2} + V_{n1}$$

$$= (-\frac{C_{t1} + C_{t2}}{C_{t1} + C_{t2}}) V_{n1} + V_{n1}$$

$$= -V_{n1} + V_{n1}$$

$$= 0$$

From the calculation, it shows that V_{n1} has no effects on the output noise.

In the second place, V_{n2} is considered and the equivalent circuit for noise source V_{n2} is shown in Fig. 7.6.

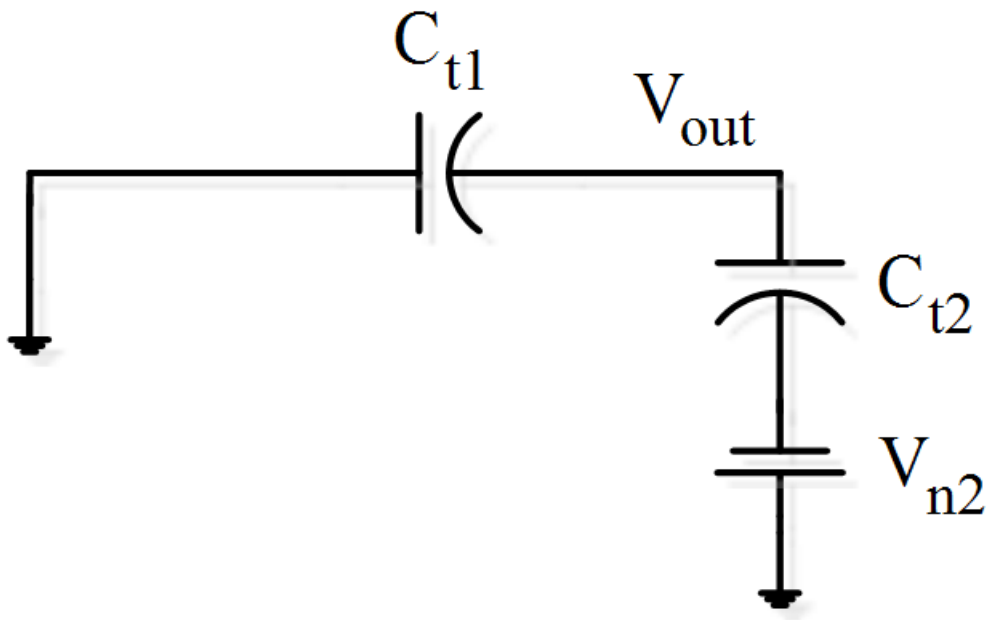


Figure 7.6 The Equivalent Circuit for Noise Source V_{n2}

$$V_{c1} = (-V_{n2}) \times (\frac{C_{t2}}{C_{t1} + C_{t2}})$$

$$V_{c2} = (-V_{n2}) \times (\frac{C_{t1}}{C_{t1} + C_{t2}})$$

V_{c1}, V_{c2} and V_{n2} are correlated. Add them together,

$$V_{tot2} = V_{c1} + V_{c2} + V_{n2}$$

$$= (-\frac{C_{t1} + C_{t2}}{C_{t1} + C_{t2}}) V_{n2} + V_{n2}$$

$$= -V_{n2} + V_{n2}$$

$$= 0$$

From the calculation, it shows that V_{n2} has no effects on the output noise.

Finally, continuous-time thermal noise V_{n3} is considered at this time and the equivalent circuit for noise source V_{n3} is shown in Fig. 7.7. This is in MSB conversion and assumes switch sizes are the same. As a result, C_{t1} and R_1 are equal to C_{t2} and R_2 respectively. However, this assumption is not true after MSB conversion. The ratio between C_{t1} and C_{t2} may vary.

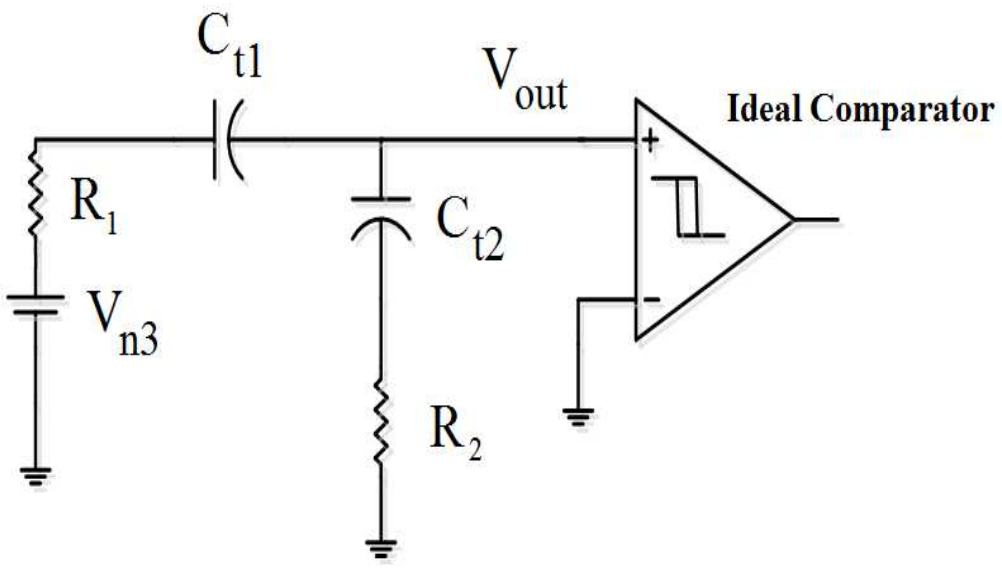


Figure 7.7 The Equivalent Circuit for Continuous-Time Noise Source V_{n3}

Power Spectra Density of thermal noise at V_{out} caused by V_{n3} can be calculated as,

$$V_{out} = V_{n3} \times \frac{1}{2} = \frac{\sqrt{4kTR_1}}{2}$$

The comparator is ideal so that bandwidth is infinite which causes the V_{n3} noise at V_{out} is also infinite. A new model is needed for comparator and it should not affect the results at V_{out} caused by noise voltage V_{n1} and V_{n2}. Noise source V_{n4} has the same situation as V_{n3}. Power Spectra Density of thermal noise at V_{out} caused by V_{n4} can be calculated as,

$$V_{out} = V_{n4} \times \frac{1}{2} = \frac{\sqrt{4kTR}}{2}$$

The noise at V_{out} caused by V_{n4} is infinite since the comparator bandwidth is infinite.

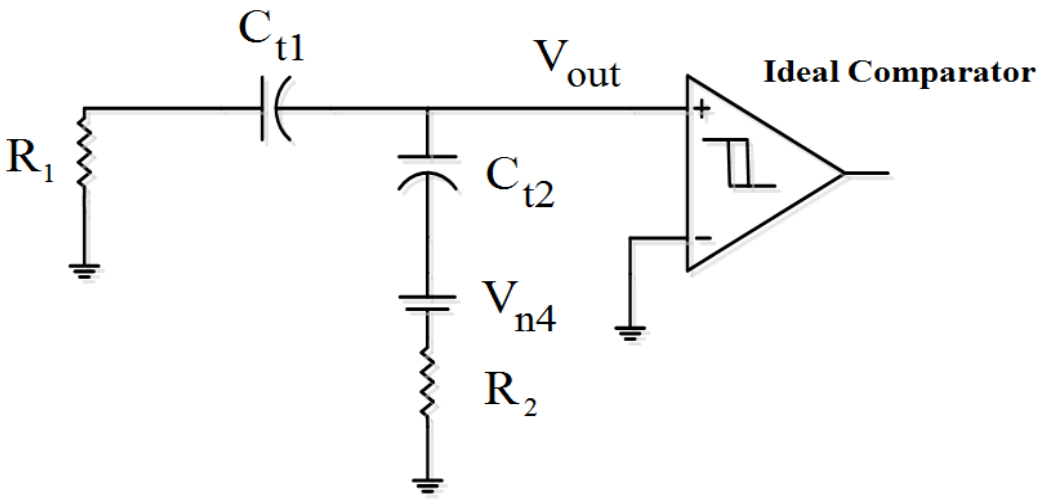


Figure 7.8 The Equivalent Circuit for Continuous-Time Noise Source V_{n4}

Model of Comparator

In order to make this analysis more practical, we created a model to replace the ideal comparator and it is shown in Fig. 7.9.

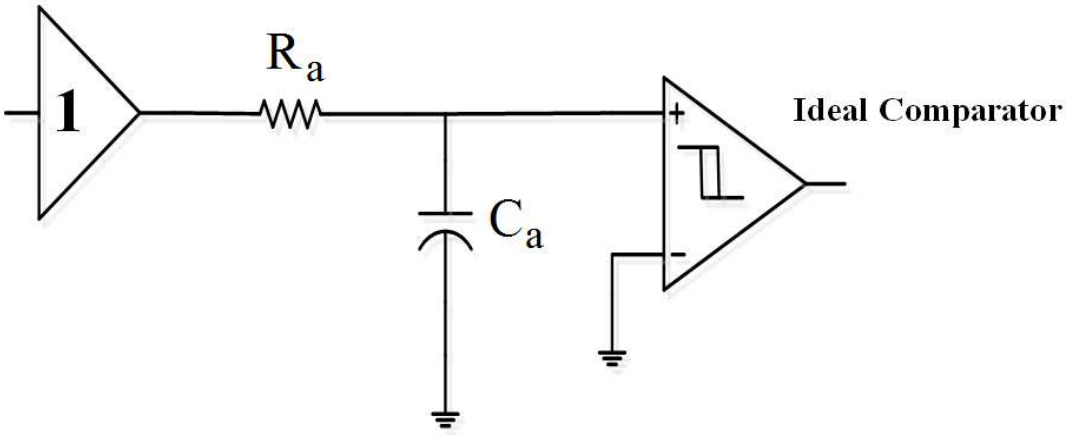


Figure 7.9 The New Model for Comparator

R_a and C_a form a low pass filter which represents the bandwidth of comparator. Before this low-pass filter, a voltage buffer is used. The reason why need a voltage buffer is that input resistance of comparator is very large. After low-pass filter, an ideal comparator is used.

Consider V_{n3} again using the new comparator model. Fig. 7.10 shows the circuit.

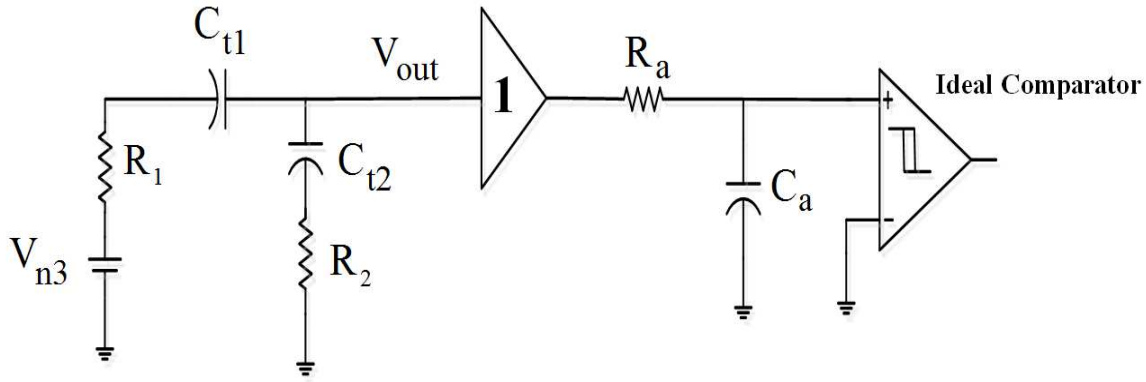


Figure 7.10 The Equivalent Circuit for Noise Source V_{n3} with the New Comparator Model

Assume RC is the time constant of capacitor DAC and R_aC_a is 10 times smaller than RC. As a result, the bandwidth of comparator is 10 times larger than the bandwidth of capacitor DAC so that capacitor DAC has enough time to settling. The thermal noise voltage at V_{out} caused by V_{n3} can be calculated as,

$$RC = R_1 C_{t1} = R_2 C_{t2} = 10 \times RaCa$$

$$v_{out} = \sqrt{\frac{1}{4} 4kTR \int_0^{\infty} \left| \frac{1}{1 + \frac{j2\pi RCf}{10}} \right|^2 df}$$

$$= \sqrt{2kTR \frac{\pi}{2} \left(\frac{10}{2\pi RC}\right)} = \sqrt{\frac{5kT}{C}}$$

$$= \sqrt{\frac{2.5kT}{C_{TOT}}}$$

C_{TOT} is the total capacitor in capacitor DAC.

Consider V_{n4} again using the new comparator model. Fig. 7.11 shows the circuit. V_{n4} is equal to V_{n3}, the thermal noise voltage at V_{out} can be calculated as,

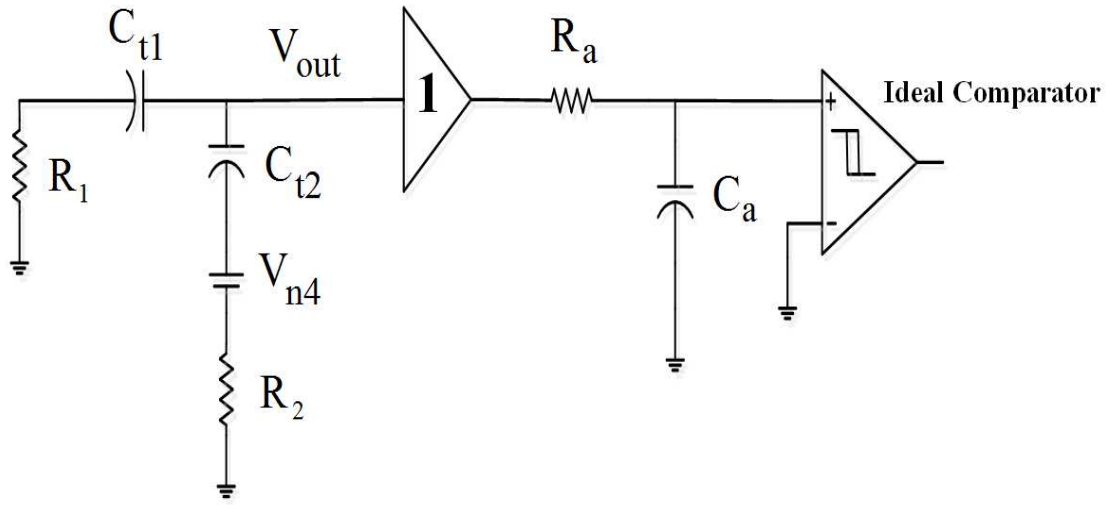


Figure 7.11 The Equivalent Circuit for Noise Source V_{n4} with the New Comparator Model

$$RC = R_1 C_{t1} = R_2 C_{t2} = 10 \times RaCa$$

$$v_{out} = \sqrt{\frac{1}{4} 4kTR \int_0^{\infty} \left| \frac{1}{1 + \frac{j2\pi RCf}{10}} \right|^2 df}$$

$$= \sqrt{2kTR \frac{\pi}{2} (\frac{10}{2\pi RC})} = \sqrt{\frac{5kT}{C}}$$

$$= \sqrt{\frac{2.5kT}{C_{TOT}}}$$

C_{TOT} is the total capacitor in capacitor DAC.

Add these two thermal noise voltage together.

$$v_n = \sqrt{\frac{2.5kT}{C_{TOT}}} + \sqrt{\frac{2.5kT}{C_{TOT}}}$$

$$= \sqrt{\frac{10kT}{C_{TOT}}}$$

C_{TOT} is the total capacitor in capacitor DAC.

This is the total thermal noise voltage at output of capacitor DAC. This noise is much higher than $\sqrt{kT / C_{TOT}}$.

7.3 Summary

From the calculation, we can find that the sampled thermal noise voltage has no effects on output noise of capacitor DAC of SAR ADC. Continuous-time thermal noise is the major contribution to the output noise of capacitor DAC of SAR ADC. Moreover, output thermal noise voltage of capacitor DAC is highly related to the bandwidth of comparator.

CHAPTER 8

CONCLUSION

A method has been introduced that uses a graphical representation of a circuit to identify positive feedback loops in order to determine the uniqueness of operating points in self-biasing circuits. A circuit-based Homotopy method was discussed that can be used to determine operating points in AMS circuits with one or more positive feedback loops. This method is useful for determining or verifying the presence or absence of multiple operating points that may have been introduced accidentally or intentionally during the design process. It can also be used to determine the effectiveness of start-up circuits.

Meanwhile, a method for making the RMS thermal noise voltage in sample-and-hold circuit independent of output capacitor is introduced. It provides a solution for reducing RMS thermal noise voltage smaller than kT/C noise.

Also, a numerical calculation of thermal noise voltage from charge-redistribution mode of SAR ADC is introduced. It provides a method for designers to calculate the thermal noise of capacitor DAC of SAR ADC more accurate and designers can make prediction of noise performance of SAR ADC very easily.

REFERENCE

[1] R.O. Nielsen and A.N. Willson, Jr., "A fundamental result concerning the topology of transistor circuits with multiple equilibria," *Proceedings of the IEEE*, vol. 68, no. 2, pp. 196-208, February 1980.

[2] I.W. Sandberg and A.N. Willson Jr., "Topological criteria for establishing the uniqueness of solutions to the DC equations of transistor networks," *IEEE Transactions on Circuit and Systems*, vol. CAS-24, no. 7, pp.349-362, July 1977.

[3] T. Nishi and L.O. Chua, "Topological criteria for nonlinear resistive circuits containing controlled sources to have a unique solution," *IEEE Transactions on Circuits and Systems*, vol. CAS-31, no. 8, pp. 722-741,August 1984.

[4] T. Nishi, "On the number of solutions of a class of nonlinear resistive circuit," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Singapore, pp. 766-769, 1991.

[5] M.M. Green, and A.N. Willson Jr., "How to identify unstable dc operating points", *IEEE TCAS-I*, vol. 39, no. 10, pp. 820-832,1992.

[6] M.M Green and R.C. Melville, "Sufficient conditions for finding multiple operating points of dc circuits using continuation methods," in *Proc. IEEE int. Symp. Circuits Systems*, May 1995, pp. 117-120.

[7] R.C. Melville, L. Trajkovic, S.-C. Fang, and L.T. Watson, "Artificial parameter homotopy methods for the dc operating point problem," *IEEE Trans. Computer-Aided Design*, vol. 12, no. 6, pp. 861-877, Jun. 1993.

[8] J.A. Bondy and U.S.R. Murty, *Graph Theory with Applications*. New York: Elsevier, 1976.

[9] D.B. West, *Introduction to Graph Theory* (Prentice-Hall, Englewood Cliffs NJ, 1996).

[10] B. Bollobas, *Graph Theory, An Introductory Course*. New York: Springer-Verlag, 1979.

[11] D. B. Johnson, “Finding all the elementary circuits of a directed graph,” *SIAM J. Comput.*, vol. 4, no. 1, pp. 77-84, Mar. 1975.

[12] Y.-T. Wang, C. Zhao, R.L. Geiger, D. Chen and S.-C Huang, "Performance verification of start-up circuits in reference generators," *IEEE Int. Midwest Symp. Circuits Systems*, pp.518521, Aug 2012.

[13] R.M. Fox and M. Nagarajan, "Multiple operating points in a CMOS log- domain filter," in *Proc. IEEE Int. Symp. Circuits Systems*, vol.3, pp.689- 692, Jul 1999.

[14] C. Zhao, J. He, S.-H. Lee, K. Peterson, R.L. Geiger and D. Chen, "Linear Vt-based temperature sensors with low process sensitivity and improved power supply headroom," in *Proc. IEEE Int. Symp. Circuits Systems*, pp.2553-2556, May 2011.

[15] Y.-T. Wang, D. Chen, and R.L. Geiger, "Effectiveness of Circuitlevel Continuation Methods for Trojan State Elimination Verification," *IEEE Int. Midwest Symp. Circuits Systems,* pp.10431046, Aug 2013

[16] Y.-T. Wang, D. Chen and R.L. Geiger, "Practical Methods for Verifying Removal of Trojan Stable Operating Points," in *Proc. IEEE Int. Symp. Circuits Systems*, pp.2586-2661, May 2013.

[17] K. Yamamura, and N. Tamura, “Finding all solutions of separable systems of piecewise-linear equations using integer programming,” *Journal of Computational and Applied Mathematics*, Vol. 236, pp. 2844–2852. 2012.

[18] S. Halgas, M. Tadeusiewicz, “Analysis of CMOS circuits having multiple DC operating points,” *Przeglad Elektrotechniczny (Electrical Review)*, pp. 40-42, May 2011.

[19] L. Han, Y. Wang, X. Zhang, Y. Dai and Y. Lu, "A simple and effective method to achieve the successful start-up of a current reference," *Journal. of Semiconductors*, vol.33, no.8, 2012.

[20] H. Wen and M.M. Green, "Use of a continuation method for analyzing startup circuits," in *Proc. IEEE Int. Symp. Circuits Systems,* pp.1527-1530, May 2010.

[21] B. Murmann, "Thermal noise in track-and-hold circuits: Analysis and simulation techniques," *IEEE Solid-State Circuits Mag.*, vol. 4, no. 2, pp. 46–54, Jun. 2012.

[22] A. Shikata, et al., "A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with Tri-Level Comparator in 40nm CMOS," *IEEE Symp. VLSI Circuits,* pp. 262-263, June 2011.

[23] M. Furuta, M. Nozawa and T. Itakura, "A 10-bit, 40MS/s, 1.21 mW Pipelined SAR ADC Using Single-Ended 1.5-bit/cycle Conversion Technique", *J. Solid-State Circuits,* vol.46, no. 6, pp. 1360-1370, Apri., 2011.

[24] R. Schreier, J. Silva, J. Steensgaard and G.C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits and Systems,* vol. 52, no. 11, pp. 2358-2368, Nov. 2005.

[25] J. Craninckx and G. van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers,* pp. 246-247, Feb. 2007.

[26] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits,* vol. 34, no. 5, pp. 599–606, May 1999.

[27] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.

[28] B. Razavi, *Design of Analog CMOS Integrated Circuits.* Boston, MA: McGraw-Hill, 2001.

[29] N. Deo, *Graph Theory With Applications to Engineering and Computer Science.* Englewood Cliffs, NJ: Prentice-Hall, 1974.

[30] T.S.K.V. Lyer, *Circuit Theory*, Tata McGraw-Hill Education, New Dehli, 2006.

[31] T. Nishi, L.O Chua, "Uniqueness of solution for nonlinear resistive circuits containing CCCS's or VCVS's whose controlling coefficients are finite." *IEEE Transactions on Circuits System* 1986; CAS-33:381-397.

[32] P.E. Allen. Class Lecture, Topic: "Single Transistor Amplifiers" School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, June, 13, 2000.

[33] J. Ogrodzki, *Circuit Simulation Methods and Algorithms*, Boca Raton, Florida: CRC Press, 1994.